SPECIFICATION
FOR
APPROVAL

( ) **Preliminary Specification**
(◆) **Final Specification**

Title	13.3” QXGA OLED

Customer	Lenovo
MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LP133QX1
Suffix	EPA1

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE
K. S. Choi / G. Manager	
REVIEWED BY	
D. G. Choi / Manager [C]	
J. H. Hwang / Manager [M]	
N. B. Choi / G. Manager [P]	
PREPARED BY	
C.J. Park / Engineer	

Products Engineering Dept.
LG Display Co., Ltd

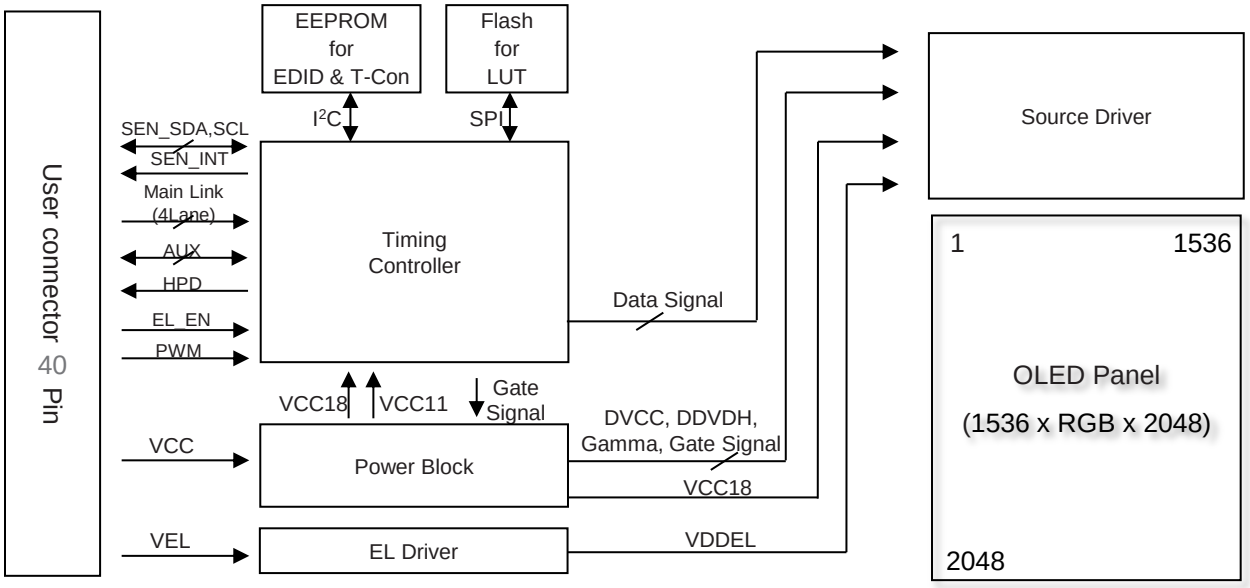
Contents

Record of Revisions

Revision No	Revision Date	Page	Before	After	EDID version
0.0	Apr. 24. 2019	All	First Draft (Preliminary Specification)	-	0.1
0.1	Jul. 12. 2019	14	f_{CLK} (214.6), t_{VP} (2108), t_{VBP} (47)	f_{CLK} (215.0), t_{VP} (2112), t_{VBP} (51) ; To optimize refresh rate 60Hz	
		16	T16 = 10ms	T16 = 40ms ; ; For EL Discharging	
		18	- Color Gamut 100% -	Update Color Tolerance to ±0.02, 0.03 Color Gamut 111% Update Viewing Angle to Max 0.07 @45˚	
		19	-	Update Condition of Gray Scale	
		39-41	Check sum “BB”	Check sum “8F”	0.2
0.2	Nov. 21. 2019	9	-	Update PWM input Capacitor	
		16	-	Update T_D	
		4, 18	-	Add Luminance @ OPR 100%	
		18	-	Update Color Coordinates (R,G,B)	
		18	Color Gamut111% (NTSC Only) Viewing angle Spec @45˚ only	Update Color Gamut 95% (Adobe, DCI-P3) Update Viewing Angle Spec @60˚	
		22,23	-	Need to Update	
		25		Update Safety	
		26	-	Label Information	
		39-41	Check sum “8F”	Check sum “17”	0.3
0.3	Jan. 16. 2020	4,6	Logic Power 1.6W	Logic Power 1.65W	
		18	Rx : 0.693, Gx : 0.185, By : 0.057	Rx : 0.695, Gx : 0.176 By : 0.056	
		22,23	-	Update Dimension	
		25	-	Update Label (Barcode L1KG→L2KG, Add MADE IN KOREA, Note1.YEAR)	
0.4	Jan. 21 2020	7	-	Add VEL Ripple Spec.	
		18	-	Update Luminance Max.	
		38-40	Check sum “17”	Check sum “EB” ; Update Color Coordinates & Year	0.4
0.5	Mar. 11 2020	4,6	Logic Power 1.65W	Logic Power 1.7W	
		7		Update PWM resolution	
		22,23	-	Update Dimension	
		25	-	Update Standards-Environment	
1.0	Apr. 22 2020	21		Update Static Folding	
		22~23		Update Dimension	
		39~40	-	APPENDIX B. LGD Proposal for System Design	
1.1	May 28 2020	22~23		Update GND and no component area	
1.2	Oct. 23 2020	41	-	APPENDIX B. LGD Proposal for PCB Shielding Guide	
1.3	Nov. 05 2020	26	-	Update Label	

1. General Description

The LP133QX1 is a Color Active Matrix Organic Light Emitting Diode Display (OLED). The matrix employs Low Temperature Poly Si Transistor as the active element. It is a top emission display type. It has a 13.3 inch diagonally measured active display area with QXGA resolution (1536 horizontal by 2048 vertical pixel array). Each pixel is divided into Red, Green and Blue sub-pixels.. Gray scale or the brightness of the sub-pixel color is determined with a 8-bit gray scale signal for each dot, thus, presenting a palette of more than 16.7M colors. The LP133QX1 has been designed to apply the interface method that enables high speed, low EMI, eDP interface with PSR. The LP133QX1 is intended to support applications where thin thickness, high contrast ratio, high color gamut. The LP133QX1 characteristics provide an excellent foldable display for Portable or Monitor mode such as tablet or notebook PC.



General Features

Active Screen Size	13.3 inches diagonal
Outline Dimension	213.80 (H, typ.) x 284.80 (V, typ.) x 0.53 (D, typ) [mm] (w/o PCB)
Pixel Pitch	0.132 mm X 0.132 mm
Pixel Format	1536 horiz. by 2048 vert. Pixels RGB Tri-angle arrangement
Color Depth	8-bit, 16.7M colors
Luminance, White	300 cd/m^2(Center 1point, Typ., OPR 80%) 240 cd/m^2(Center 1point, Typ., OPR 100%)
Power Consumption	Total 10.44W (Typ.) Logic : 1.7W (Typ. @ Mosaic), EL : 8.74W (Typ. @ Full White)
Weight	120g (Max.)(w/o Protect Film)
Bending Radius	3R (Typ.)
Surface Treatment	Glare, Hard coat (6H Cover Window Only) and Anti Fingerprint
RoHS Compliance	YES
BFR / PVC / As Free	YES
eDP version(T-con)	eDP1.3
DPCD version	Ver1.2

PSR	MBO	DPST	sDRRS	SSC	NVSR	G-sync or Free sync
Support	Not support	Not support	Not support	Support	Not support	Not support

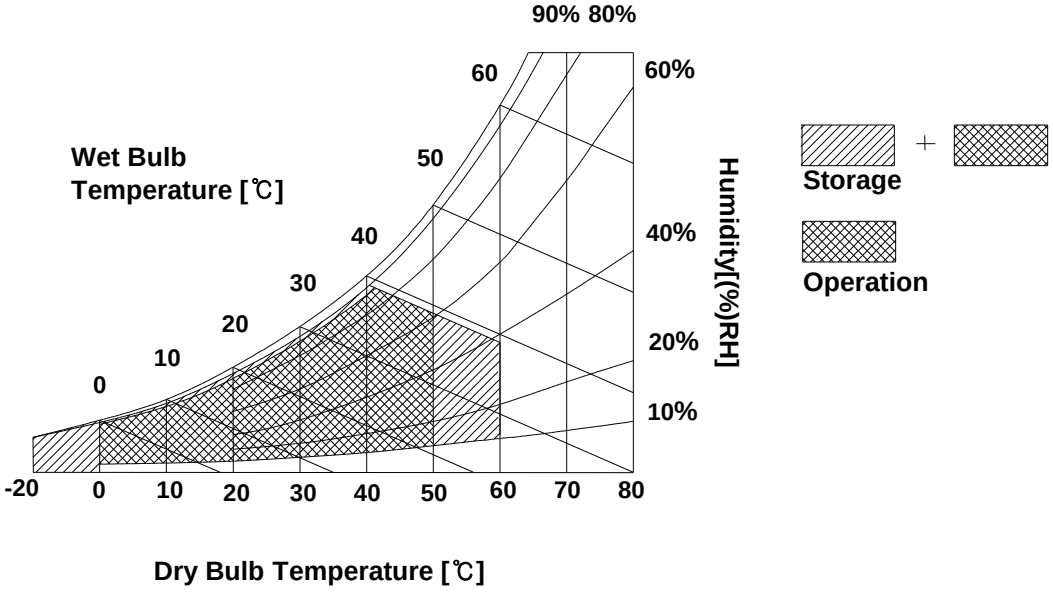
2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Values		Units	Notes
		Min	Max		
Power Input Voltage	VCC	-0.3	4.0	V_{DC}	at 25 ± 2°C
Operating Temperature	TOP	0	50	°C	1
Storage Temperature	TST	-20	60	°C	1,2
Operating Ambient Humidity	HOP	10	90	%RH	1
Storage Humidity	HST	10	90	%RH	1,2

Note : 1. Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39°C Max, and no condensation of water.
Note : 2. Storage Condition is guaranteed with unfolding under packing condition.



3. Electrical Specifications

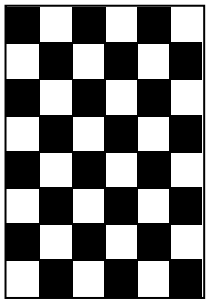
3-1. OLED Electrical Characteristics

Table 2. ELECTRICAL CHARACTERISTICS

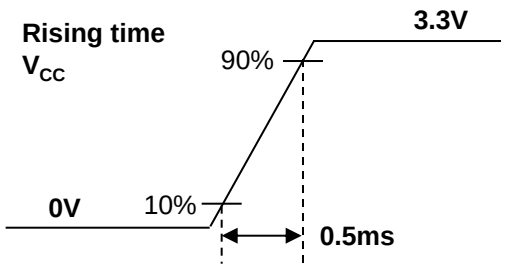
Parameter		Symbol	Values			Unit	Notes
			Min	Typ	Max		
Power Supply Input Voltage		V_{CC}	3.0	3.3	3.6	V	1
Permissive Power Supply Input Ripple		V_{CCrp}	-	-	100	mV_{p-p}	
Power Supply Input Current	Mosaic	I_{CC}	-	515	605	mA	2
Power Consumption		P_{CC}	-	1.7	2.0	W	
Power Supply Inrush Current		I_{CC_P}	-	-	2.5	A	3
Differential Impedance		Z_{eDP}	90	100	110	Ω	

Note)

1. The measuring position is the connector of Module and the test conditions are under 25℃, fv = 60Hz
2. The specified I_{CC} current and power consumption are under the V_{CC} = 3.3V , 25℃, fv = 60Hz condition and Mosaic pattern. (without Burning Compensation)



3. The V_{CC} rising time is same as the minimum of T1 at Power on sequence.



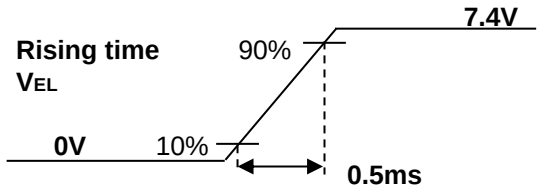
3-2. EL Electrical Characteristics

Table 3. EL ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Values			Unit	Notes
			Min	Typ	Max		
EL Power Input Voltage		V_{EL}	4.8	7.4	9.0	V	1
Permissive EL Power Input Ripple		V_{ELrp}	-	-	100	mV_{p-p}	
EL Power Input Current		I_{EL}		1180	1475	mA	2
EL Power Consumption		P_{EL}		8.74	11.0	W	
EL Power Inrush Current		I_{EL_P}	-	-	5.0	A	3
PWM Duty Ratio			1	-	100	%	4
PWM resolution				8		bit	5
PWM Frequency		F_{PWM}	200	-	1000	Hz	6
PWM	High Level Voltage	V_{PWM_H}	2.5	-	3.6	V	
	Low Level Voltage	V_{PWM_L}	0	-	0.3	V	
	Rising Time	Tr_{PWM}	-	-	500	ns	
	Falling Time	Tf_{PWM}	-	-	500	ns	
EL_EN	High Voltage	$V_{EL\_EN\_H}$	2.5	-	3.6	V	
	Low Voltage	$V_{EL\_EN\_L}$	0	-	0.3	V	
Life Time (B10)			-	15,000	-	Hrs	7

Note)

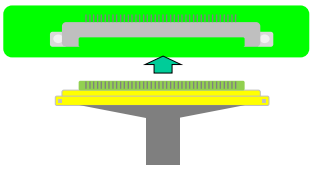
1. The measuring position is the connector of OLED Module and the test conditions are under 25℃.
2. The current and power consumption with EL Driver are under the V_{EL} = 7.4V , 25℃, PWM Duty 100% and White pattern(OPR 100%, 240nit) with the normal frame frequency operated(60Hz)
   This model apply to enable PLC(Peak Luminance Control)
3. The V_{EL} rising time is same as the minimum of T13 at Power on sequence.



4. The operation of EL Driver below minimum dimming ratio may cause flickering or reliability issue.
5. 8bit resolution means it's possible to change PWM duty by 0.4% step.
6. This Spec. is not effective at 100% dimming ratio as an exception because it has DC level equivalent to 0Hz. In spite of acceptable range as defined, the PWM Frequency should be fixed and stable for more consistent brightness control at any specific level desired.
7. The life time is determined as the time at which brightness of OLED is 50% compare to that of minimum value specified in table 7. under general user condition.

3-3. Interface Connections

Table 4. MODULE CONNECTOR PIN CONFIGURATION (CN11)

Pin	Symbol	Description	Notes
1	VCC_logic	logic and driver power	
2	VCC_logic	logic and driver power	
3	VCC_logic	logic and driver power	
4	VCC_logic	logic and driver power	
5	SEN_INT	Sensing command	
6	SEN_SCL	Sensing command	
7	SEN_SDA	Sensing command	
8	GND	High Speed Ground	
9	LANE3_N	Complement Signal Link Lane 3	
10	LANE3_P	True Signal Link Lane 3	
11	GND	High Speed Ground	
12	LANE2_N	Complement Signal Link Lane 2	
13	LANE2_P	True Signal Link Lane 2	
14	GND	High Speed Ground	
15	LANE1_N	Complement Signal Link Lane 1	[Connector] Hirose, KN38A-40S-0.5H (40pin, 0.5pitch) or equivalent
16	LANE1_P	True Signal Link Lane 1	
17	GND	High Speed Ground	
18	LANE0_N	Complement Signal Link Lane 0	
19	LANE0_P	True Signal Link Lane 0	
20	GND	High Speed Ground	
21	AUX_CH_P	True Signal Auxiliary Channel	[Connector pin arrangement] Pin 40 Pin 1 
22	AUX_CH_N	Complement Signal Auxiliary Channel	
23	GND	High Speed Ground	
24	HPD	HPD signal pin	
25	EL_EN	EL on/off control	
26	EL_PWM	System PWM signal input for dimming	
27	BIST or NC	Panel Self Test Enable (Optional)	
28	GND	EL ground	
29	GND	EL ground	
30	GND	EL ground	
31	GND	EL ground	
32	NC	Reserved for OLED manufacturer's use	
33	VEL	EL power (7.4V Typical)	
34	VEL	EL power (7.4V Typical)	
35	VEL	EL power (7.4V Typical)	
36	VEL	EL power (7.4V Typical)	
37	VEL	EL power (7.4V Typical)	
38	VEL	EL power (7.4V Typical)	
39	VEL	EL power (7.4V Typical)	
40	VEL	EL power (7.4V Typical)	

Note) This pin-map is not VESA Standard but customized map.

3-3-1. Input/output signal circuit

Figure1.HPD Output circuit is as below

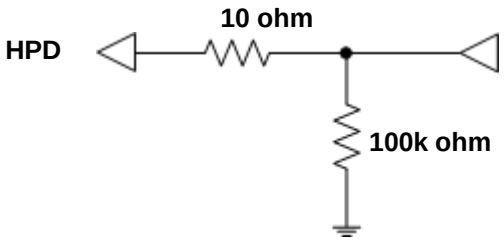


Figure2.EL PWM input circuit is as below

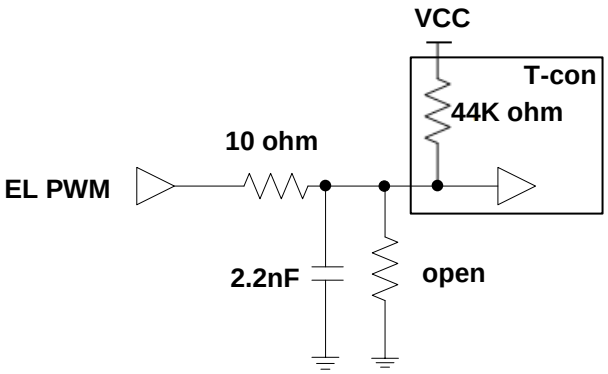


Figure3.EL Enable input circuit is as below

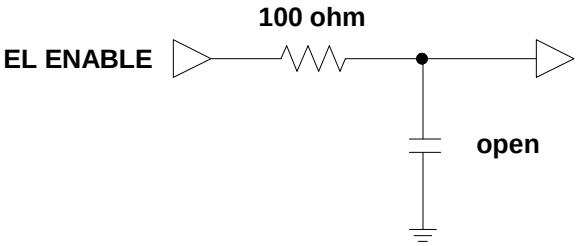
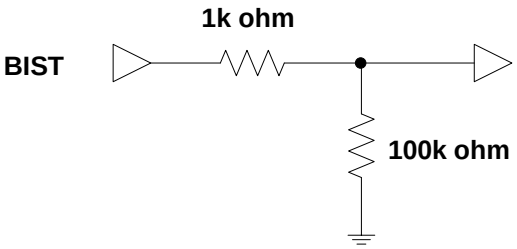
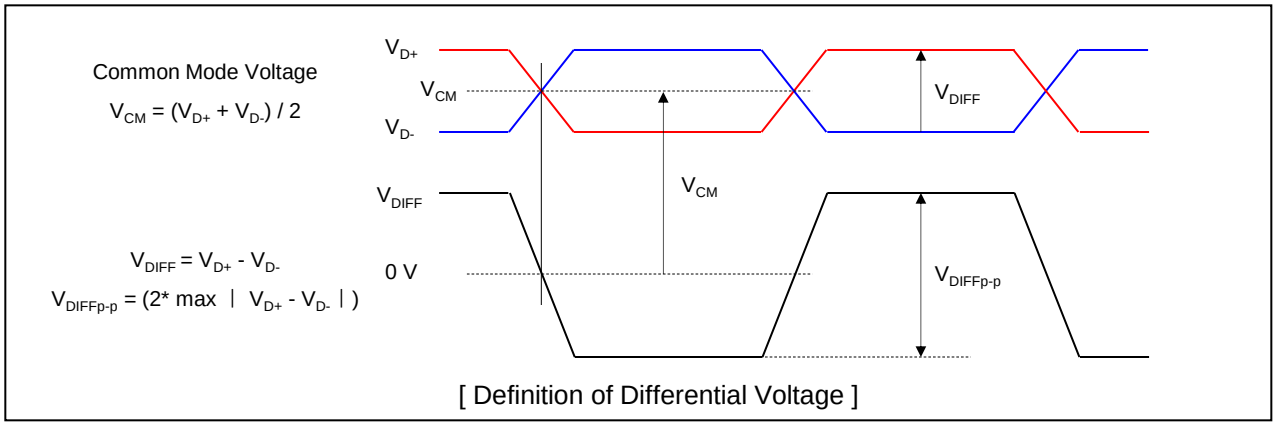


Figure4.BIST input circuit is as below



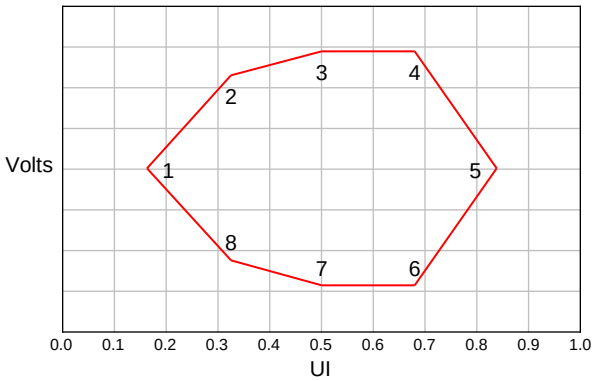
3-4. eDP Signal Timing Specifications

3-4-1. Definition of Differential Voltage

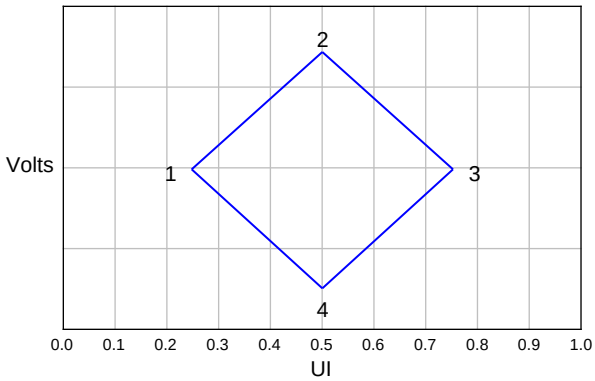


[Definition of Differential Voltage]

3-4-2. Main Link EYE Diagram



[EYE Mask at Source Connector Pins]



[EYE Mask at Sink Connector Pins]

Point	Reduced Bit Rate		High Bit Rate	
	Time(UI)	Voltage(V)	Time(UI)	Voltage(V)
1	0.127	0.000	0.210	0.000
2	0.291	0.160	0.355	0.140
3	0.500	0.200	0.500	0.175
4	0.709	0.200	0.645	0.175
5	0.873	0.000	0.790	0.000
6	0.709	-0.200	0.645	-0.175
7	0.500	-0.200	0.500	-0.175
8	0.291	-0.160	0.355	-0.140

[EYE Mask Vertices at Source Connector Pins]

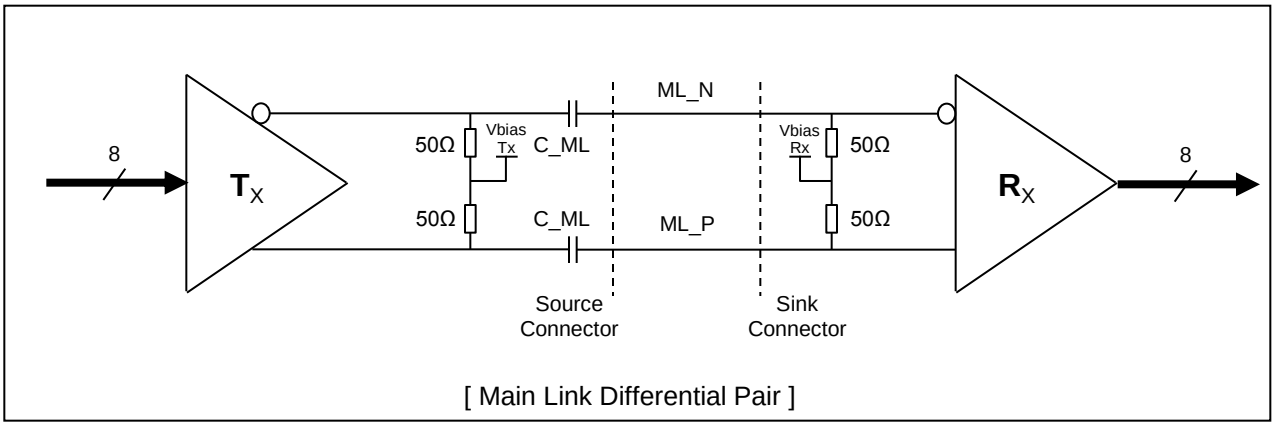
Point	Reduced Bit Rate		High Bit Rate	
	Time(UI)	Voltage(V)	Time(UI)	Voltage(V)
1	0.375	0.000	0.246	0.000
2	0.500	0.023	0.500	0.075
3	0.625	0.000	0.755	0.000
4	0.500	-0.023	0.500	-0.075

[EYE Mask Vertices at Sink Connector Pins]

Point	Reduced Bit Rate		High Bit Rate	
	Time(UI)	Voltage(V)	Time(UI)	Voltage(V)
1	0.270	0.000	0.246	0.000
2	0.500	0.068	0.500	0.075
3	0.731	0.000	0.755	0.000
4	0.500	-0.068	0.500	-0.075

[EYE Mask Vertices at embedded DP Sink Connector Pins]

3-4-3. eDP Main Link Signal

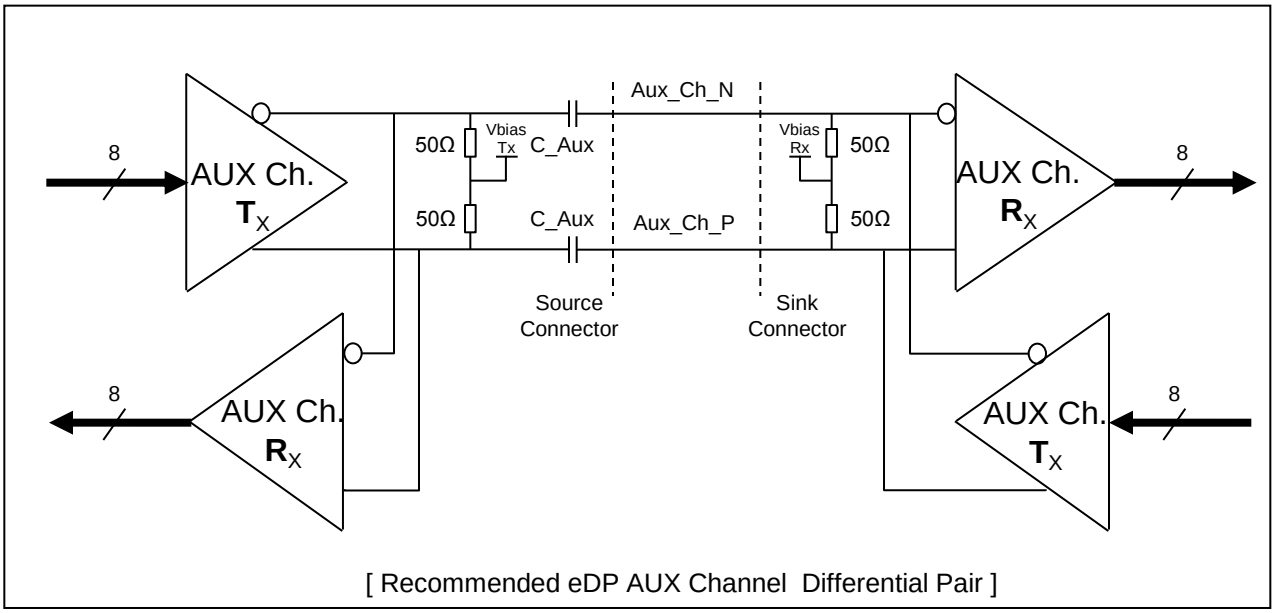


[Main Link Differential Pair]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval for high bit rate (2.7Gbps / lane)	UI_HBR	-	370	-	ps	
Unit Interval for reduced bit rate (1.62Gbps / lane)	UI_RBR	-	617	-	ps	
Link Clock Down Spreading	Amplitude	0	-	0.5	%	
	Frequency	30		33	kHz	
Differential peak-to-peak voltage at Source side connector	$V_{TX-DIFFp-p}$	350	-	-	mV	For HBR(2.7Gbps)
		400	-	-		For RBR(1.62Gbps)
EYE width at Source side connector	$T_{TX-EYE-CONN}$	0.58	-	-	UI	For HBR(2.7Gbps)
		0.75	-	-	UI	For RBR(1.62Gbps)
Differential peak-to-peak voltage at Sink side connector	$V_{RX-DIFFp-p}$	150	-	-	mV	For HBR(2.7Gbps)
		136	-	-		For RBR(1.62Gbps)
EYE width at Sink side connector	$T_{RX-EYE-CONN}$	0.51	-	-	UI	For HBR(2.7Gbps)
		0.46	-	-	UI	For RBR(1.62Gbps)
Rx DC common mode voltage	$V_{RX\ CM}$	0	-	2	V	
AC Coupling Capacitor	C_{SOURCE_ML}	75		200	nF	Source side

Note)
1. Termination resistor is typically integrated into the transmitter and receiver implementations.
2. AC Coupling Capacitor is not placed at the sink side.
3. In cabled embedded system, it is recommended the system designer ensure that EYE width and voltage are met at the sink side connector pins.

3-4-4. eDP AUX Channel Signal

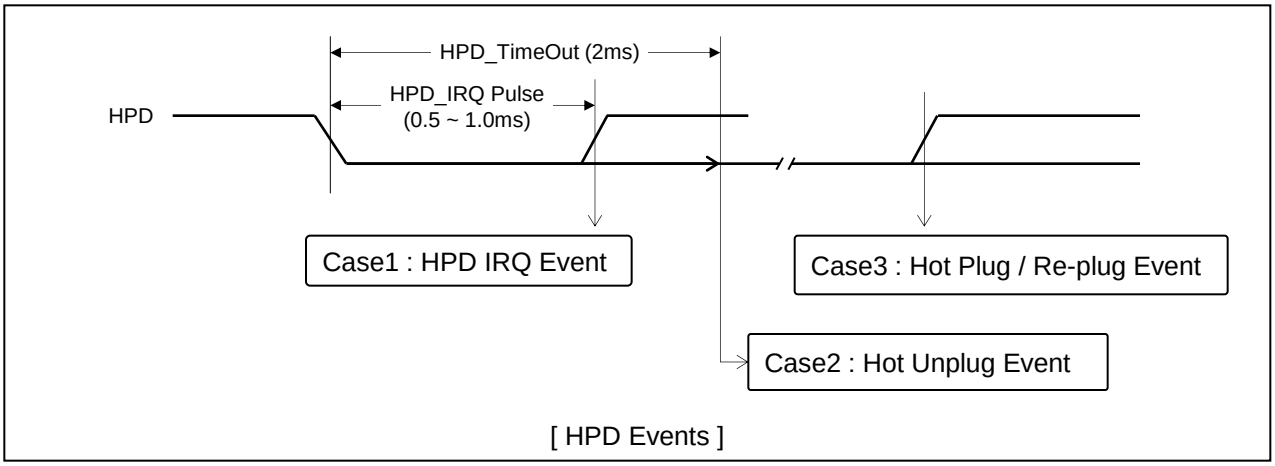


[Recommended eDP AUX Channel Differential Pair]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
AUX Unit Interval	UI	0.4	-	0.6	us	
AUX Jitter at Tx IC Package Pins	T_{jitter}	-	-	0.04	UI	Equal to 24ns
AUX Jitter at Rx IC Package Pins		-	-	0.05	UI	Equal to 30ns
AUX Peak-to-peak voltage at Connector Pins of Transmitting	$V_{AUX-DIFFp-p}$	0.39	-	1.38	V	
AUX Peak-to-peak voltage at Connector Pins of Receiving		0.36	-	1.36	V	
AUX EYE width at Connector Pins of Tx and Rx		0.98	-	-	UI	
AUX DC common mode voltage	V_{AUX-CM}	0	-	1.0	V	
AUX AC Coupling Capacitor	$C_{SOURCE-AUX}$	75		200	nF	Source side

Note)
1. Termination resistor is typically integrated into the transmitter and receiver implementations.
2. AC Coupling Capacitor is not placed at the sink side.
3. $V_{AUX-DIFFp-p} = 2^* | V_{AUXP}-V_{AUXN} |$

3-4-5. eDP HPD Signal



[HPD Events]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
HPD Voltage	HPD	2.25	-	3.6	V	Sink side Driving
Hot Plug Detection Threshold		2.0	-	-	V	Source side Detecting
Hot Unplug Detection Threshold		-	-	0.8	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1.0	ms	
HPD_TimeOut		2.0	-	-	ms	HPD Unplug Event

Note)
1. HPD IRQ : Sink device wants to notify the Source device that Sink's status has changed so it toggles HPD line, forcing the Source device to read its Link / Sink Receiver DPCD field via the AUX-CH
2. HPD Unplug : The Sink device is no longer attached to the Source device and the Source device may then disable its Main Link as a power saving mode
3. Plug / Re-plug : The Sink device is now attached to the Source device, forcing the Source device to read its Receiver capabilities and Link / Sink status Receiver DPCD fields via the AUX-CH

3-5. Signal Timing Specifications

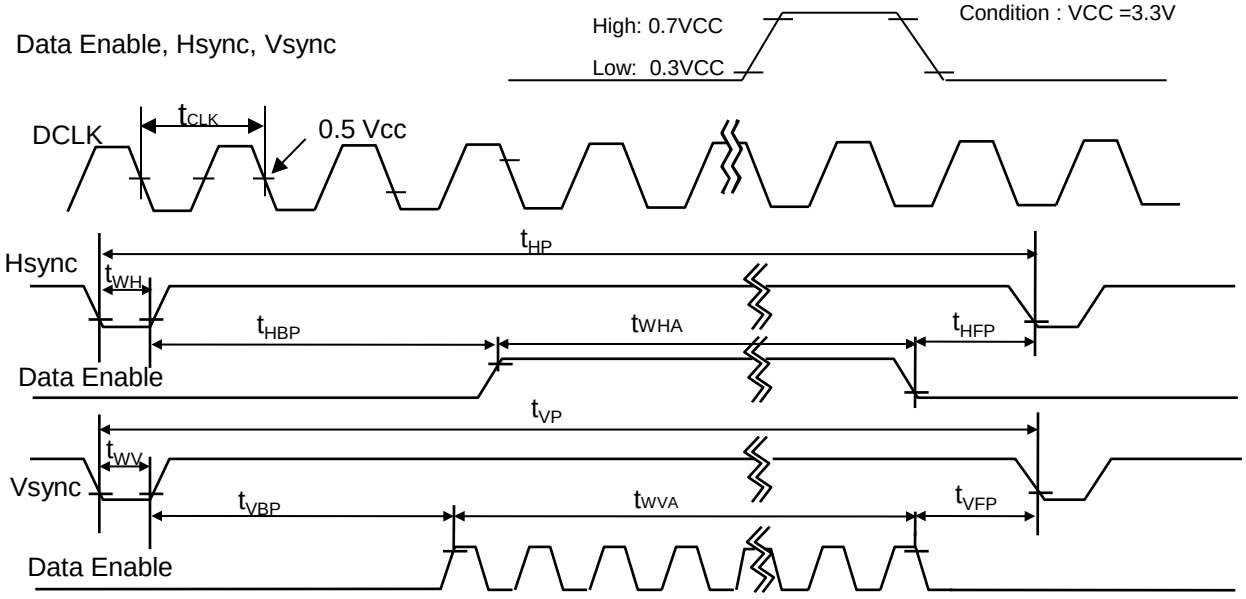
This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications and specifications of eDP Tx/Rx for its proper operation.

Table 4. TIMING TABLE

ITEM	Symbol		Min	Typ	Max	Unit	Note
DCLK	Frequency	f_{CLK}	-	215.0	-	MHz	
Hsync	Period	t_{HP}	-	1696	-	t_{CLK}	
	Width	t_{WH}	-	32	-		
	Width-Active	t_{WHA}	1536				
Vsync	Period	t_{VP}	-	2112	-	t_{HP}	
	Width	t_{WV}	-	10	-		
	Width-Active	t_{WVA}	2048				
Data Enable	Horizontal back porch	t_{HBP}	-	80	-	t_{CLK}	
	Horizontal front porch	t_{HFP}	-	48	-		
	Vertical back porch	t_{VBP}	-	51	-	t_{HP}	
	Vertical front porch	t_{VFP}	-	3	-		

Notice. All reliabilities are specified for timing specification based on refresh rate of 60Hz.

3-6. Signal Timing Waveforms



3-7. Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color ; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 5. COLOR DATA REFERENCE

Color		Input Color Data																							
		RED								GREEN								BLUE							
		MSB							LSB	MSB							LSB	MSB							LSB
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED (0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	…					…								…								…			
	RED (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN (0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	...					…								…								…			
	GREEN (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	GREEN (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
BLUE	BLUE (0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	…					…								…								…			
	BLUE (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	BLUE (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

3-8. Power Sequence

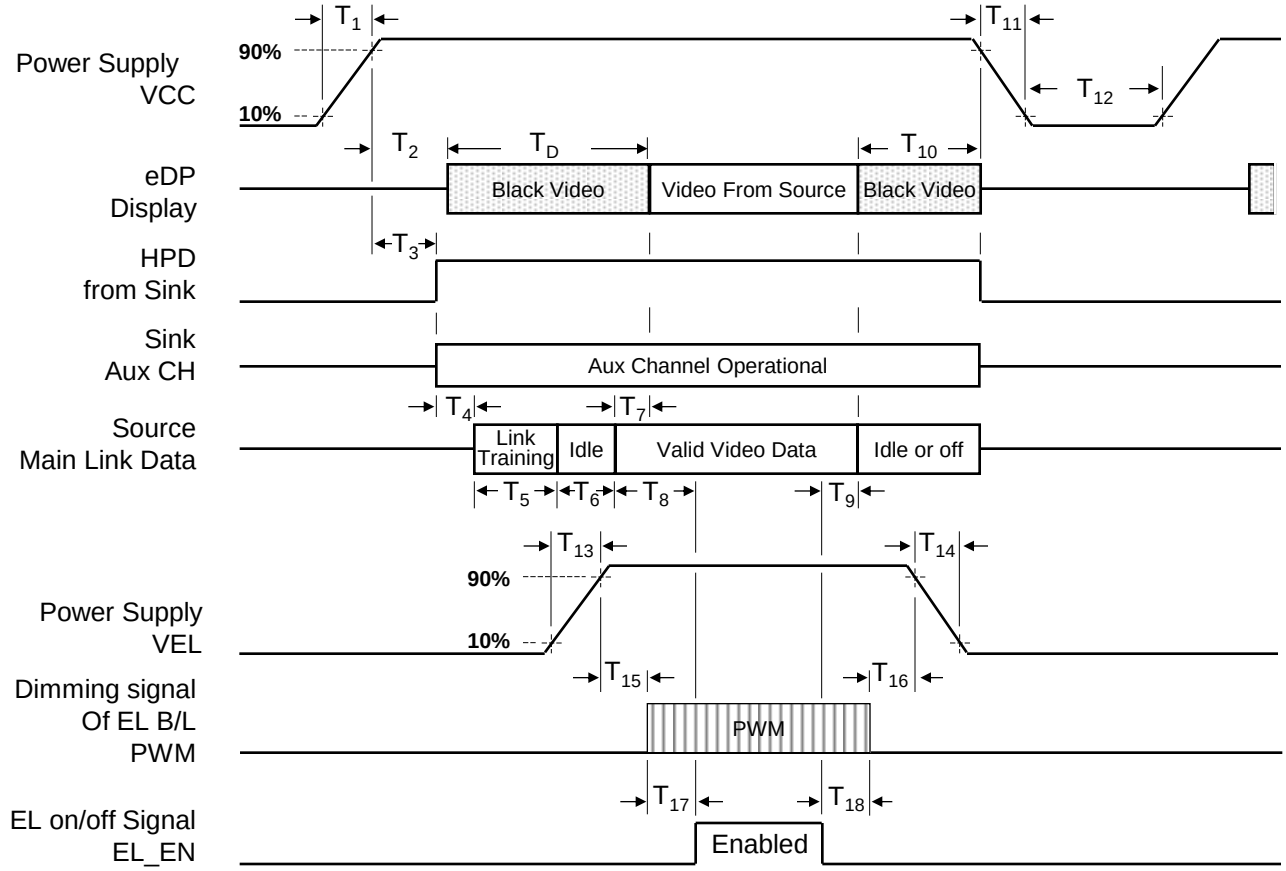


Table 6. POWER SEQUENCE TABLE

Symbol	Required By	Limits		Units	Notes
		Min	Max		
T_1	Source	0.5	10	ms	-
T_2	Sink	600	-	ms	-
T_3	Sink	0	500	ms	-
T_4	Source	-	-	ms	-
T_5	Source	-	-	ms	-
T_6	Source	-	-	ms	-
T_7	Sink	0	50	ms	-
T_8	Source	-	-	ms	LGD recommend Min 200ms
T_9	Source	-	-	ms	

Symbol	Required By	Limits		Units	Notes
		Min	Max		
T_{10}	Source	0	500	ms	-
T_{11}	Source	-	10	ms	-
T_{12}	Source	500	-	ms	-
T_{13}	Source	0.5	10	ms	-
T_{14}	Source	0.5	10	ms	-
T_{15}	Source	10	-	ms	-
T_{16}	Source	40	-	ms	-
T_{17}	Source	0	-	ms	-
T_{18}	Source	0	-	ms	-
T_D	Sink		1700	ms	Compensation Enable case

Note) 1. Do not insert the mating cable when system turn on.
2. Valid Data have to meet "3-3. eDP Signal Timing Specifications"
3. Video Signal, EL_EN and PWM need to be low condition on invalid status.
4. LGD recommend the rising sequence of VEL after the Vcc and valid status of Video Signal turn on.

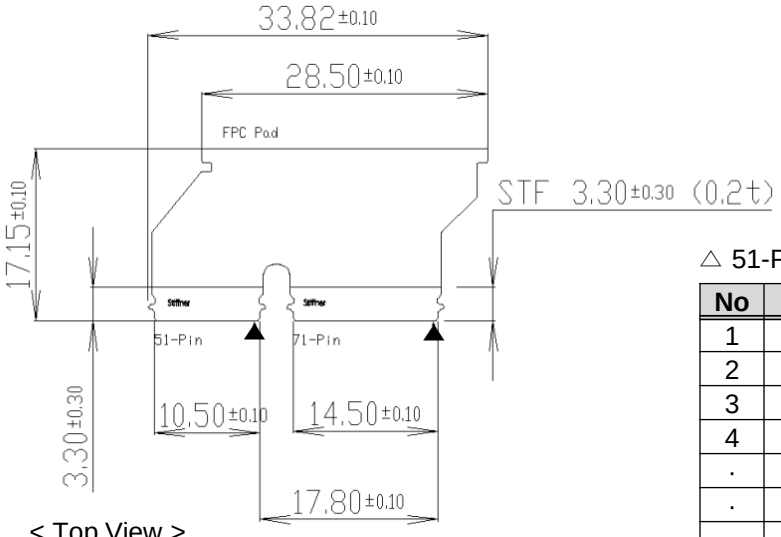
3-9. Touch General Specification

The contents provide general characteristics for the model LP133QX1.

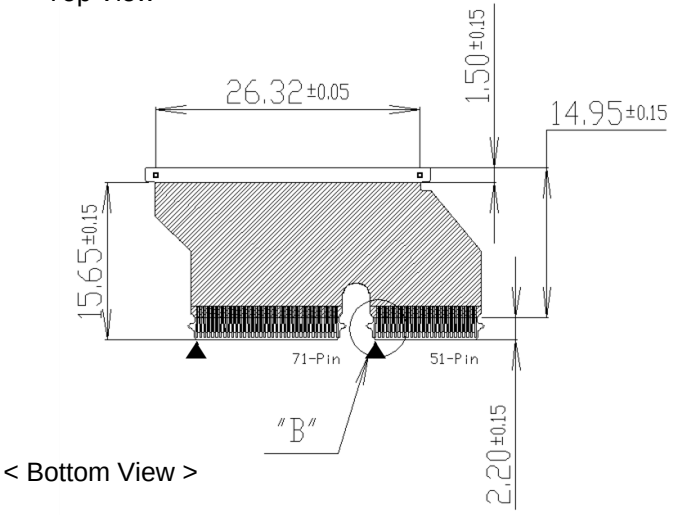
	Item		Spec
General Specification	System		Mutual Capacitance Type
	Sensor	Type.	Advanced On-Cell Touch
		Sensor Channel Pitch	4.488mm (X) x 4.488mm (Y)
	Number of Sensor Channel		61ea (X) x 46ea (Y)

Note)
1. Touch design and performance is optimized to W9017 (Wacom G14T)
2. Wacom AES 1.0 & WHLK is supported by co-working with Customer

3-9-1. Touch FPC & Pin-map



< Top View >



< Bottom View >

△ 51-Pin

No	Name
1	GND
2	Tx00
3	Tx01
4	Tx02
.	.
.	.
.	.
46	Tx44
47	Tx45
48	GND
49	GND
50	GND
51	GND

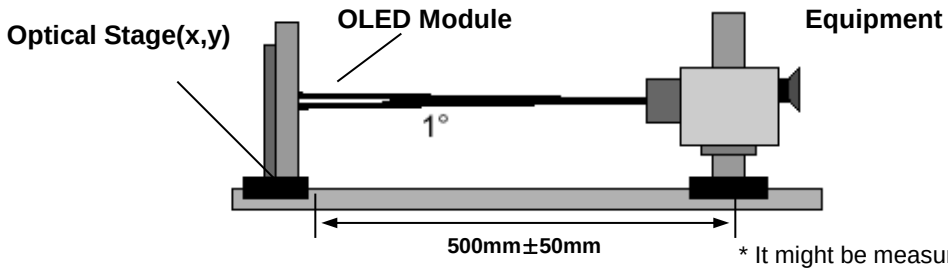
△ 71-Pin

No	Name
1	GND
2	GND
3	GND
4	GND
5	Rx00
6	Rx01
7	Rx02
.	.
.	.
.	.
64	Rx59
65	Rx60
66	GND
67	GND
68	GND
69	GND
70	GND
71	GND

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 20 minutes in a dark environment at 25°C. The values specified are at an approximate distance 50cm from the OLED surface at a viewing angle of Φ and Θ equal to 0°.
FIG. 1 presents additional information concerning the measurement equipment and method.

FIG. 1 Optical Characteristic Measurement Equipment and Method



* It might be measured by landscape mode

Table 7. OPTICAL CHARACTERISTICS Ta=25°C, VCC=3.3V, fv=60Hz

Parameter		Symbol	Values			Units	Notes
			Min	Typ	Max		
Contrast Ratio		CR	5000	-	-		1
Surface Luminance, white (OPR 80%)		L_{WH}	270	300	330	cd/m²	2
Surface Luminance, white (OPR 100%)		L_{WH}	216	240	264	cd/m²	2
Luminance Variation		$\delta_{WHITE\ (5P)}$	80	-	-	%	3
		$\delta_{WHITE(13P)}$	60	-	-		
Response Time		Tr + Tf	-	2	-	ms	4
Color Coordinates	RED	Rx	- 0.030	0.695	+ 0.030	-	5
		Ry		0.305			
	GREEN	Gx		0.176			
		Gy		0.740			
	BLUE	Bx		0.140			
		By		0.056			
	WHITE	Wx	-0.020	0.313	+0.020		
		Wy		0.329			
Color Gamut	NTSC	-	-	111	-	%	Area Ratio (CIE 1931)
	Adobe			95			Covering Ratio (CIE 1931)
	DCI-P3			95			
Viewing Angle	x axis, right(Φ=0°)	-	-	85	-	Degree	6
	x axis, left (Φ=180°)	-	-	85	-		
	y axis, up (Φ=90°)	-	-	85	-		
	y axis, down (Φ=270°)	-	-	85	-		
Viewing Angle (color)	θ= 45° / 60° (R,L,U,D)	ΔXY	-	0.05	0.07	-	7
Gray Scale (Gamma)		-	-	2.2	-	-	8

Note)

1. It should be measured in the center of screen(1 Point). Contrast Ratio(CR) is defined mathematically as

$$\text{Contrast Ratio(1 Point)} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

2. Surface luminance is the center of screen(1 Point, Typ) across the OLED surface 50cm from the surface with 80% pixels displaying white. For more information see FIG 2.
   This model apply to enable PLC(Peak Luminance Control).

L_{WH} = 1 Point, Typ

* OPR : Open Pixel Ratio

3. The variation in surface luminance , The panel total variation (δ WHITE) is determined by measuring N at each test position 1 through 13 and then defined as following numerical formula.
   For more information see FIG 2.

$$\delta \text{ WHITE (5P)} = \frac{\text{Minimum (1,2, … 5 Point)}}{\text{Maximum (1,2, … 5 Point)}} \qquad \delta \text{ WHITE (13P)} = \frac{\text{Minimum (1,2, … 13 Point)}}{\text{Maximum (1,2, … 13 Point)}}$$

4. Response time is the time required for the display to transition from black to white (rise time, Tr) and from white to black (falling time, Tf) at first peak. For additional information see FIG 3.

5. It should be measured in the center of screen (1Point).

6. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the OLED surface. For more information see FIG 4.

7. Difference between color coordinates of front (Wx0,Wy0), (Rx0,Ry0), (Gx0,Gy0), (Bx0,By0) and color coordinates of viewing angle (Wxn, Wyn), (Rxn, Ryn), (Gxn, Gyn), (Bxn, Byn)

$$\text{Delta xy } (\triangle xy) = \sqrt{(Wxn-Wx0)^2 + (Wyn-Wy0)^2}$$

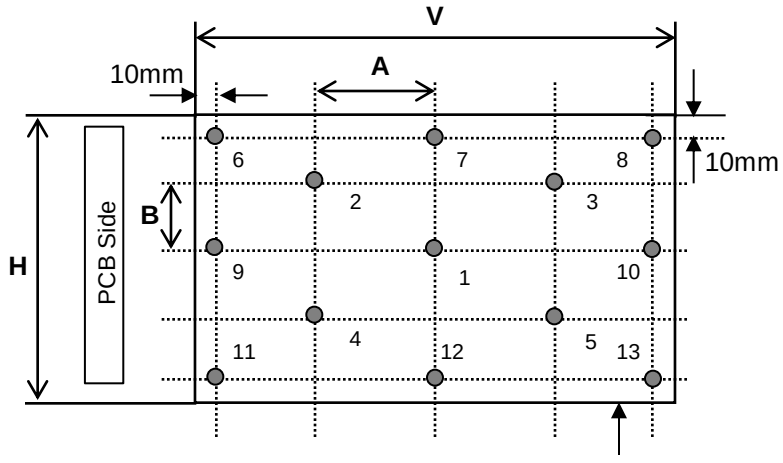
8. Gray scale specification under OPR 80%

Gray Level0	Luminance [%] (Typ)
L0	0.0
L31	0.9
L63	4.4
L95	10.9
L127	21.3
L159	35.0
L191	52.5
L223	74.1
L255	100.0

Gamma 2.2 for gray scale more than 16/255 Gray

FIG. 2 Luminance

<Measuring point for Luminance & measuring point for Luminance variation>



H,V : ACTIVE AREA
A : H/4 mm
B : V/4 mm
POINTS: 13 POINTS

FIG. 3 Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white” at first peak

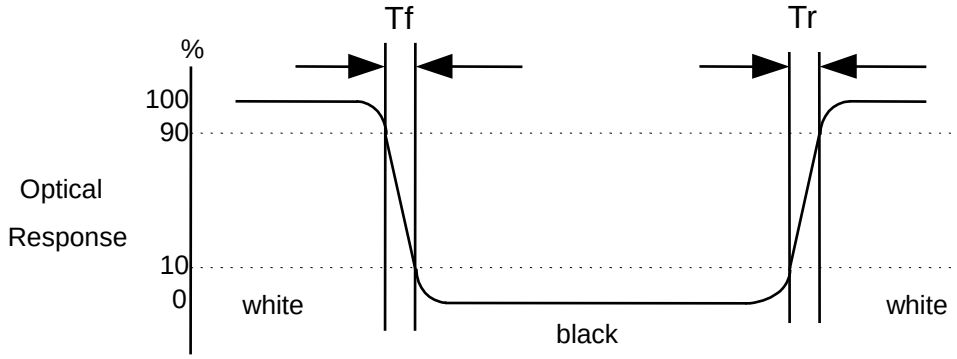
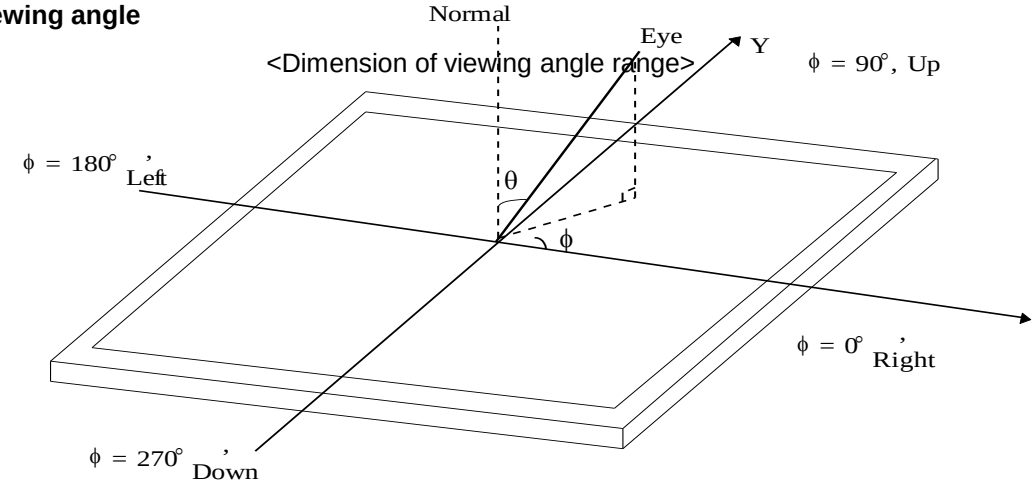


FIG. 4 Viewing angle

<Dimension of viewing angle range>

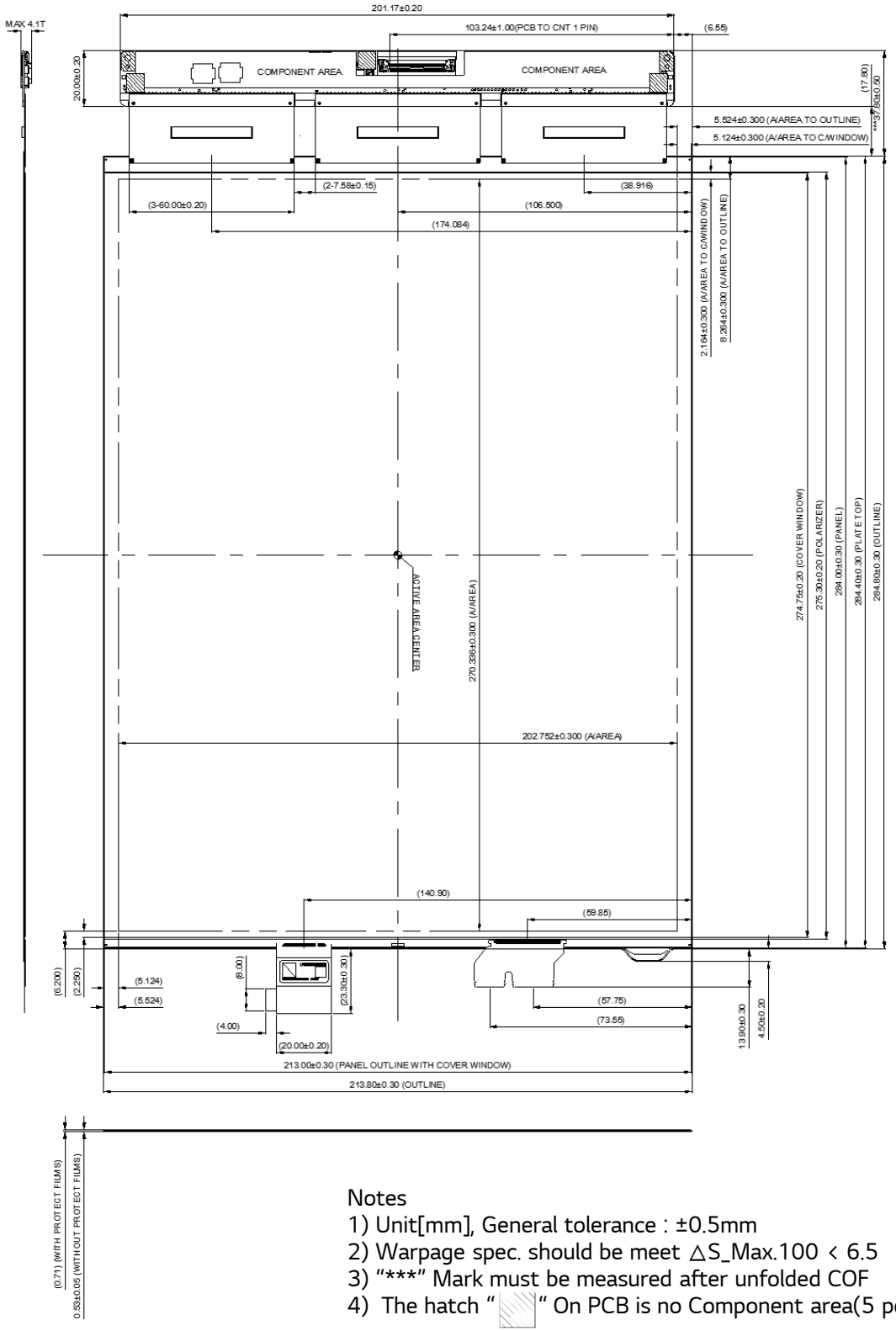


5. Mechanical Characteristics

The contents provide general mechanical characteristics for the model LP133QX1. In addition the figures in the next page are detailed mechanical drawing of the OLED.

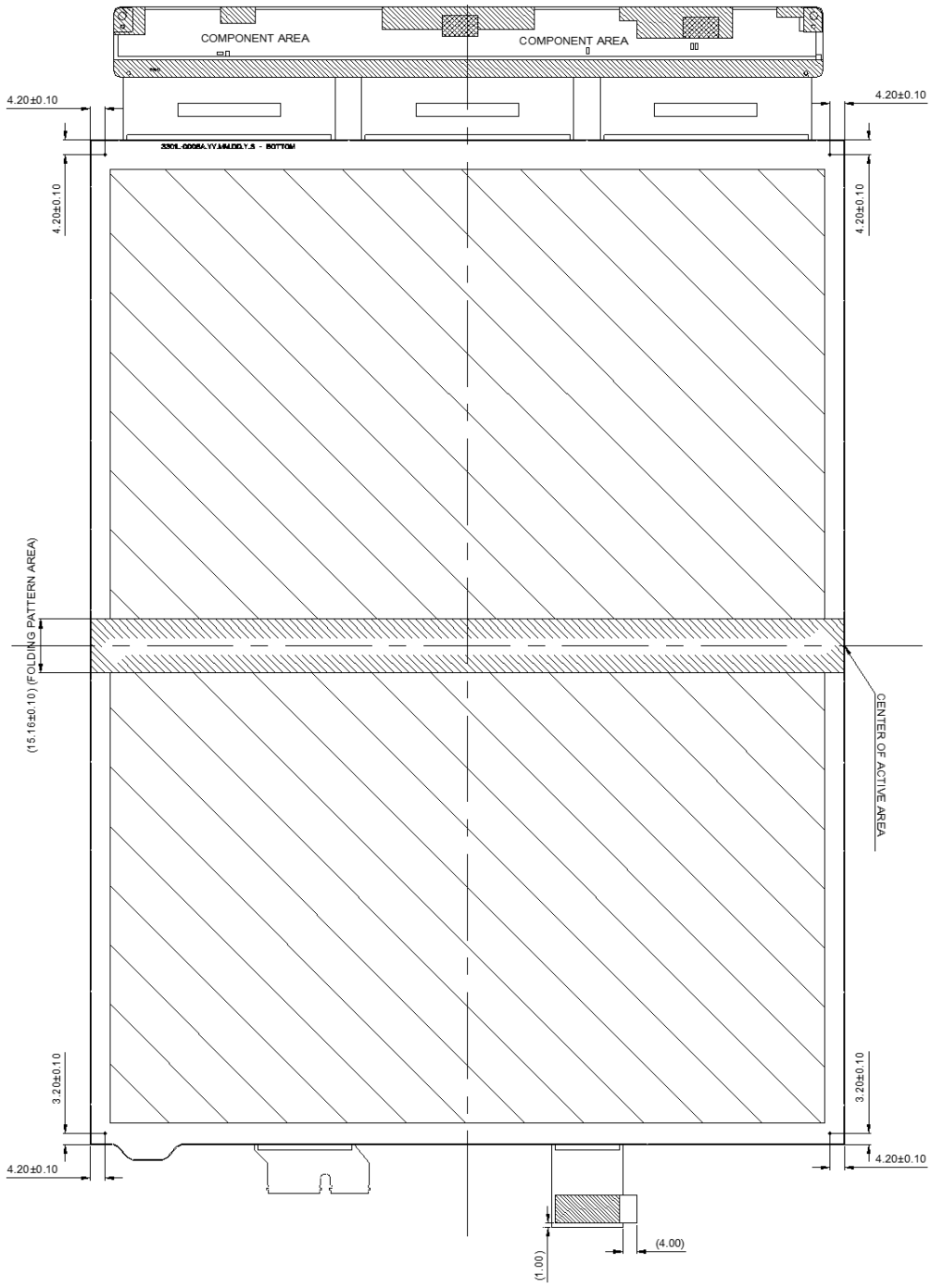
Outline Dimension (without PCB)	Horizontal	213.8 ± 0.3 mm
	Vertical	284.8 ± 0.3 mm
	Thickness	0.53 ± 0.05 mm
Active Display Area	Horizontal	202.752 ± 0.3 mm
	Vertical	270.336 ± 0.3 mm
Weight	120g (Max.) (w/o Protect Film)	
Bending Radius	3R (+0.4/-0.2, w/o abnormal stress)	
Dynamic Folding	50,000 times (Close to open 2sec, Open to close 2sec, closed holding 5sec) at Room Temperature/humidity with LGD Jig. After 24hr leave with full open, defect should be nothing except waviness level.	
Static Folding	180deg folded for 30 days at Room Temperature/humidity with LGD Jig. After 24hr leave with full open, The judgment criteria is based on the waviness level that Customer and LGD conferred.	
Surface Treatment	Glare, Hard coat (6H Cover Window Only) and Anti Fingerprint	

<FRONT VIEW>



Notes
1) Unit[mm], General tolerance : ±0.5mm
2) Warpage spec. should be meet △S_Max.100 < 6.5
3) "***" Mark must be measured after unfolded COF
4) The hatch " " On PCB is no Component area(5 points)

<REAR VIEW>



Notes
1) Unit[mm], General tolerance : ±0.5mm

2) The hatch " " On PCB is no Component area (6 points)

3) The hatch " " On PCB is GND area (2 points)

6. Reliability

Environment test condition with unfold

No.	Test Item	Conditions
1	High temperature storage test	Ta= 60°C, 240h
2	Low temperature storage test	Ta= -20°C, 240h
3	High temperature operation test	Ta= 50°C, 50%RH, 240h
4	Low temperature operation test	Ta= 0°C, 240h
5	Altitude operating storage / shipment	0 ~ 10,000 feet (3,048m) 24Hr 0 ~ 40,000 feet (12,192m) 24Hr
6	ESD with LGD Test Jig	± 8kV for contact discharge ± 15kV for air discharge

[Result Evaluation Criteria]

1. Comparing the initial functional FOS status, there should be no major change which might affect the practical display function when the display reliability test is conducted.

2. After conduct reliability tests, LGD guarantees only functional FOS quality.

3. In the Reliability Test, Confirm performance after leaving in room temp.

4. In the standard condition, there shall be no practical problems that may affect the display function 24 hours later after reliability test. After the reliability test, we can guarantee the product only when the corrosion is causing its malfunction. The corrosion causing no functional defect can not be guaranteed.

7. International Standards

7-1. Safety

a) IEC 62368-1, The International Electro-technical Commission(IEC).
Audio/video, Information and Communication Technology Equipment - Safety - Safety Requirements.

b) EN 62368-1, European Committee for Electro-technical Standardization (CENELEC)
Audio/video, Information and Communication Technology Equipment - Safety Requirements

c) UL 62368-1, UL LLC.
Audio/video, Information and Communication Technology Equipment - Safety Requirements

d) CAN/CSA C22.2 No.62368-1, Canadian Standards Association (CSA).
Audio/video, Information and Communication Technology Equipment - Safety Requirements

e) IEC 60950-1, The International Electro technical Commission (IEC).
Information Technology Equipment - Safety - Part 1 : General Requirements

7-2. Environment

a) RoHS, Directive 2011/65/EU of the European Parliament and of the council of 8 June 2011

8. Packing

8-1. Designation of Lot Mark

L3KG : Module Fab @ Gumi, Korea

L1KP : Module Fab @ Paju, Korea

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)
E : MONTH
D : YEAR
F ~ M : SERIAL NO.

Note

1. YEAR

Year	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025
Mark	F	G	H	J	K	L	M	N	P	Q

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial No. is printed on the label. The label is attached on front side of Vss GND FPC.
This is subject to change without prior notice.

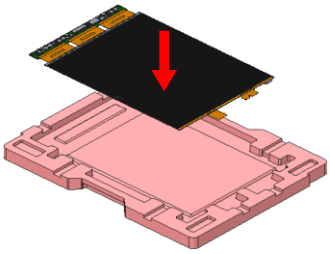
8-2. Packing Form

a) Package quantity in one box : 7 pcs

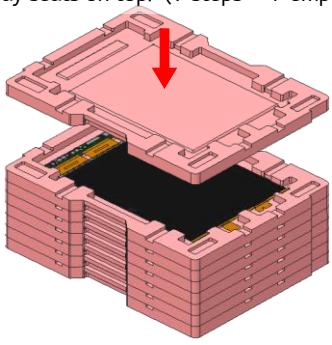
b) Box Size : 417 x 317 x 170 mm

8-3. Packing Assembly

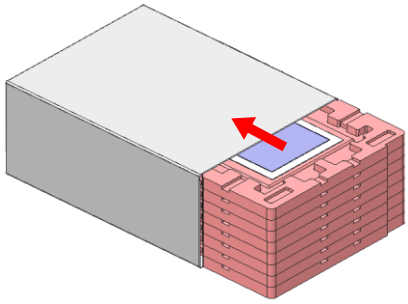
1. Placement on Tray(1EA/Tray)



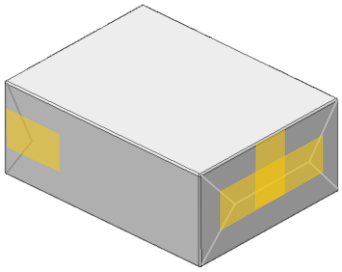
2. After loading in the forward direction in 7 steps,
Empty tray seats on top. (7 steps + 1-empty tray)



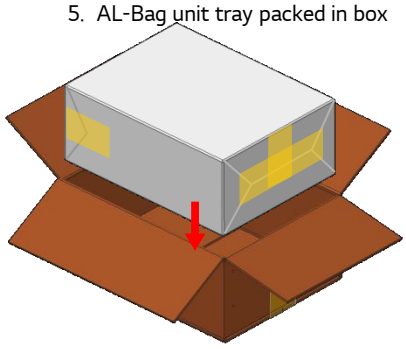
3. Put 2ea of desiccant on the top tray,
All AL-Bag Packing



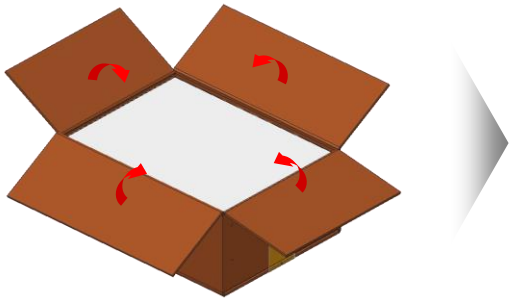
4. AL-Bag taping closed
after pulling out the remaining area.

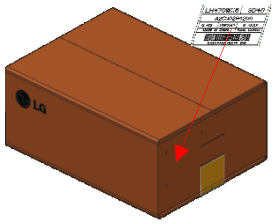


5. AL-Bag unit tray packed in box



6. Box closed and attach one box label to the outer designated position

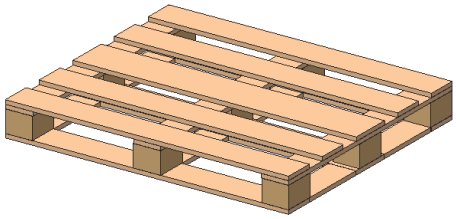




7. Finish by taping.

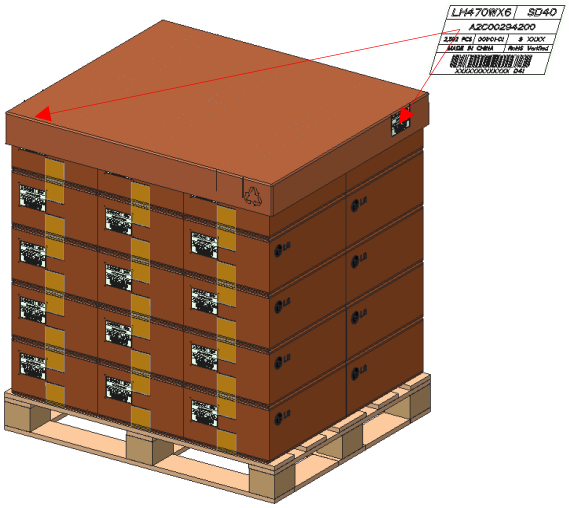
8-4. Pallet Assembly

1. Pallet Ready

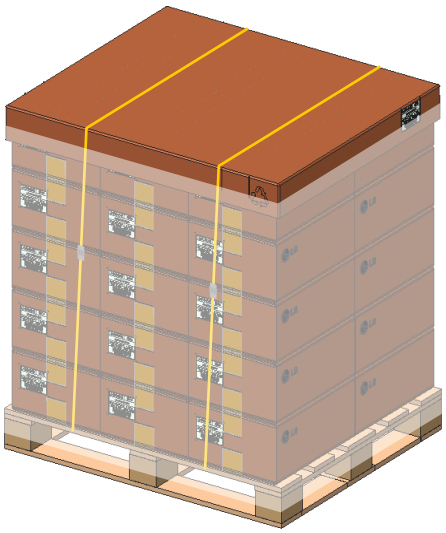


2. 3 x 2 x 5 Box Pattern

3. Angle Cover & Pallet Label 2EA



4. Banding & Wrapping



9. PRECAUTIONS

Please pay attention to the followings when you use this OLED module.

9-1. LAMINATION PRECAUTIONS

(1) You should consider the laminating structure so that uneven force (ex. Twisted stress) is not applied to the folding area of module. And the case on which a module is laminated should have sufficient strength so that external force is not transmitted directly to the module.
(2) Do not treat the module with excessive force. The COF, Touch FPC and VSS GND should not be bent by force. And keep the module and PCB horizontally.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(8) When handling the OLED module, it needs to handle with care not to give mechanical stress to the PCB and Folding area."
(9) Module back-side adhesive attach guide refer to the Appendix A.

9-2. OPERATING PRECAUTIONS

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=± 200mV(Over and under shoot voltage)

(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.

9-3. ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and OLED.

9-5. STORAGE

When storing modules as spares for a long time, the following precautions are necessary.

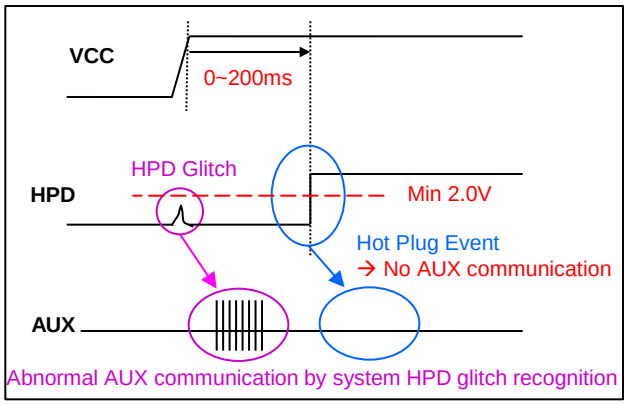
(1) Store them with unfold in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity with AL bag & desiccant up to 3 month.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

9-6. HANDLING PRECAUTIONS FOR PROTECTION FILM

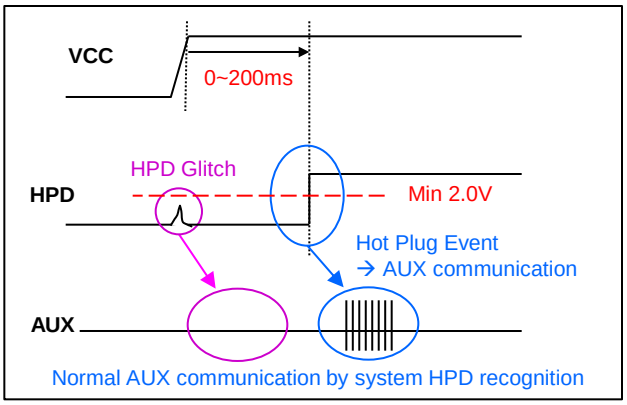
(1) You must use pulling tape when the protection film is peeled off.
(2) When the protection film is peeled off, static electricity is generated the film as well as polarizer and back-side silicone surface. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(3) The protection film is attached to the polarizer with a small amount of glue.
If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt to remain on the polarizer.
Please carefully peel off the protection film without rubbing it against the polarizer.
(4) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer and back-side surface after the protection film is peeled off.
(5) You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.
(6) You can remove the glue on back-side surface to using sticky roller.
(7) Strong caution must be taken not to deform the module when peeling off the protection film.
(8) Do not fold the module before peeling off the polarizer protection film.
(9) After peeling off the polarizer protection films, do not attach anything such as protectors or stickers on the polarizer surface.

APPENDIX A. LGD Proposal for eDP Interface Design Guide

1	HPD Signal recognition



[Abnormal Communication By HPD Glitch]

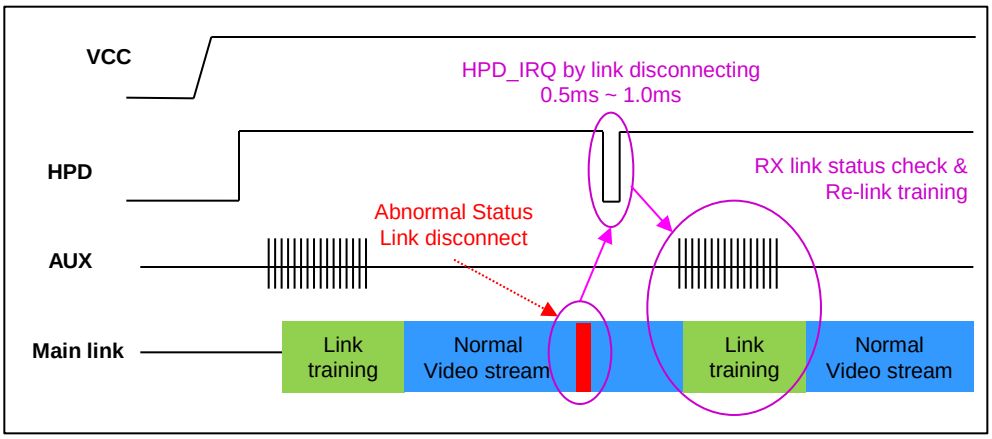


[Normal Communication By HPD Signal]

Define	1. Hot Plug Detection (HPD) Threshold level of Source Device is minimum 2.0V
	2. HPD Unplug : HPD pulse stays low longer than 2ms. DP Tx shall wait for HPD signal to go high again.
	3. “HPD High” is confirmed only after HPD has been asserted continuously for 100msec.

2	IRQ (Interrupt Request) HPD Pulse Definition

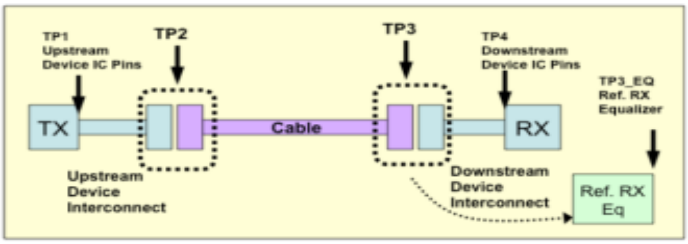
Ex) HPD Pulse



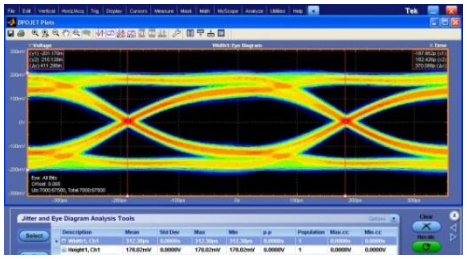
Define	Upon detection this “HPD IRQ Event”(0.5ms ~ 1ms) ,the source device must read the link / sink status field of the DPCD and take corrective action.

APPENDIX A. LGD Proposal for eDP Interface Design Guide

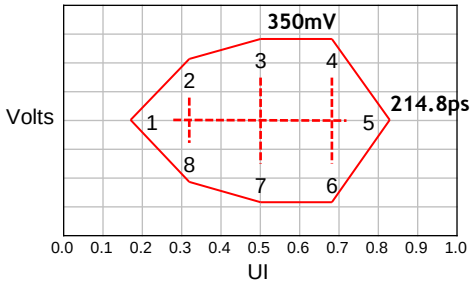
3 Main Link EYE Diagram



*Note : In PCBA side, LGD measured TP3 on connector

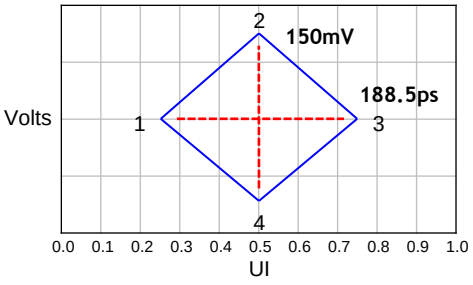


[EYE Diagram]



Point	UI	Voltage (Volts)
1	0.210	0.000
2	0.355	0.140
3	0.500	0.175
4	0.645	0.175
5	0.790	0.000
6	0.645	-0.175
7	0.500	-0.175
8	0.355	-0.140

[EYE Vertices for TP2 at HBR]

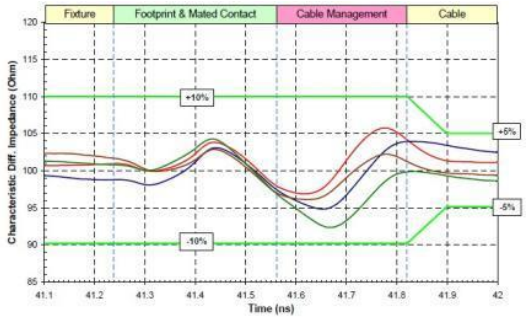


Point	UI	Voltage (Volts)
1	0.246	0.000
2	0.500	0.075
3	0.755	0.000
4	0.500	-0.075

[EYE Vertices for TP3 at HBR]

Define	Main Link EYE Diagram should meet TP2 and TP3 point

4 Cable Impedance management

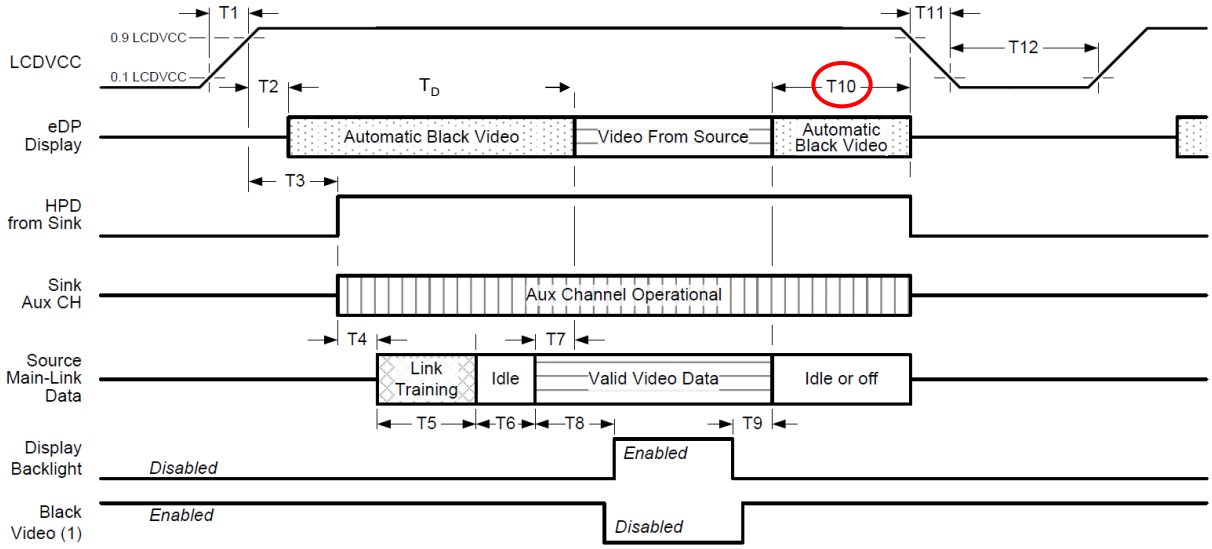


Segment	Differential Impedance	Maximum Tolerance
Fixture	100 Ω	+/- 10%
Connector	100 Ω	
Wire management	100 Ω	
Cable	100 Ω	+/- 5%

Define	Cable Impedance 100 Ω +/- 5% (95Ω ~ 105Ω)

APPENDIX A. LGD Proposal for eDP Interface Design Guide

5	Main Link Off vs. Power Off at Non-PSR



Timing Parameter	Description	Required By	Min	Max
T10	Delay from end of valid video from Source to Power Off	Source	0ms	500ms

* LGD recommend that Source must power off the VCC if Main Link off like below.

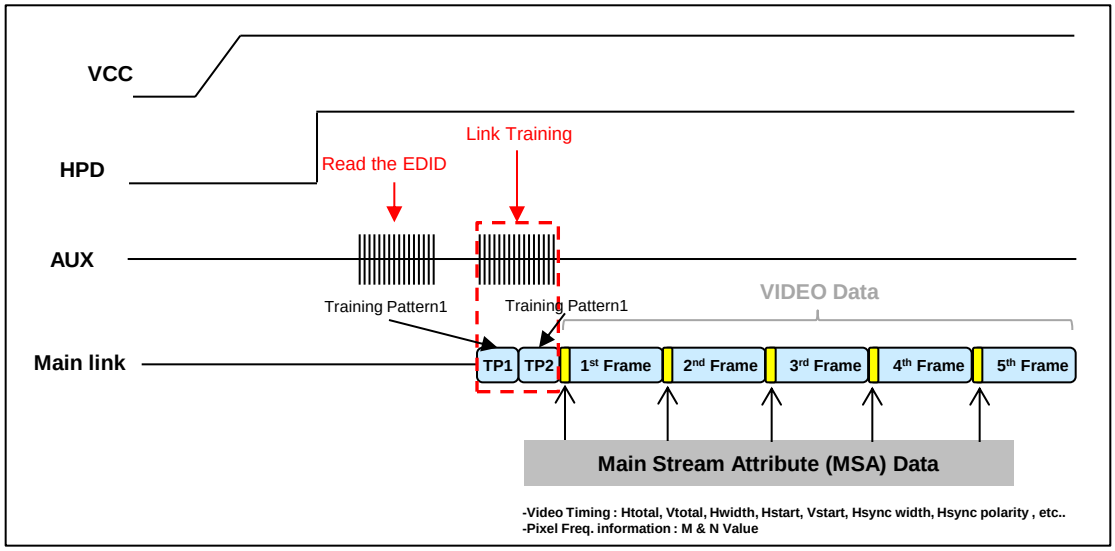
[Case1. Resolution Change]

[Case2. Close the Lid]

Define	If Main Link off signal from Source, then VCC must be Power Off within T10 period at Non-PSR mode

APPENDIX A. LGD Proposal for eDP Interface Design Guide

6	Main Link M & N value of MSA data

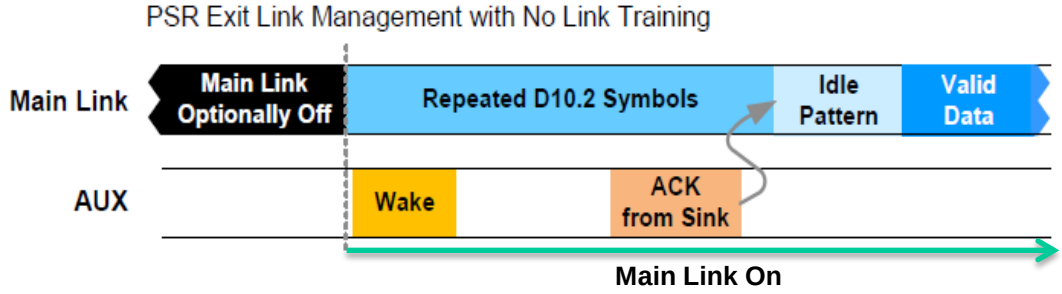


Define	It need to fix M& N value of MSA data output to prevent the initial abnormal M& N Value from incoming after power on.

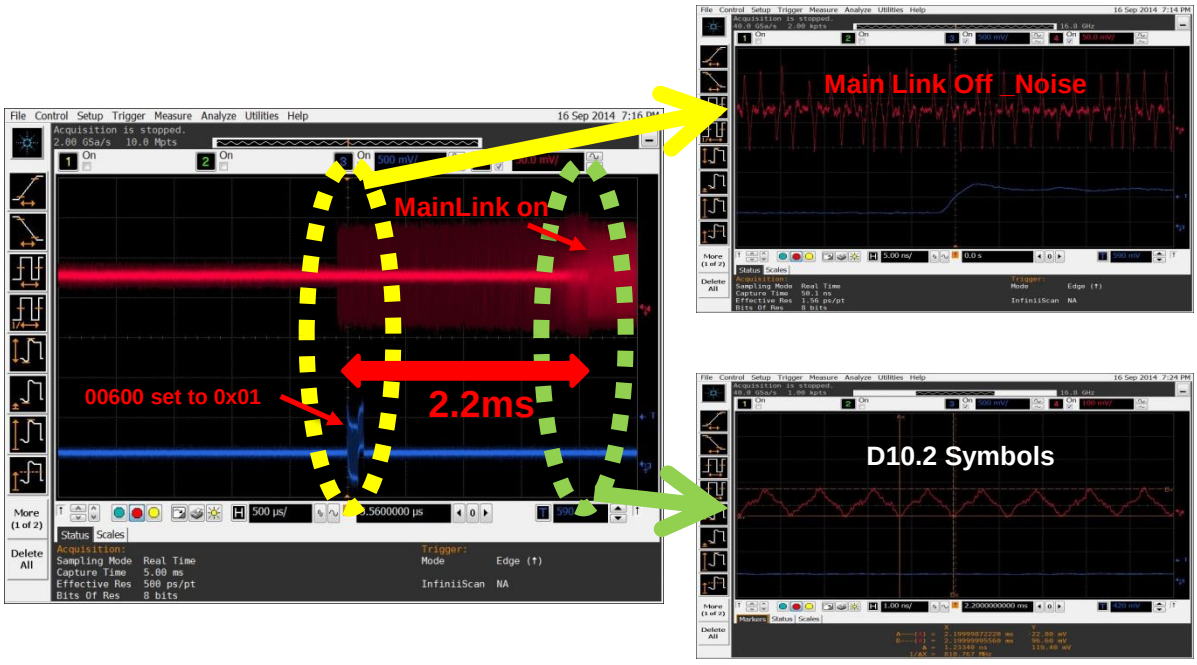
APPENDIX A. LGD Proposal for eDP Interface Design Guide

7	PSR Exit

If link training is not required, the Source must begin transmitting data on the Main Link prior to the wake AUX command which occurs through writing 01h to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h; see *DP v1.2a*), as illustrated in the upper portion of Figure 6-9. This transmitted data must be a repetition of D10.2 symbols (which is the same as Link Training Pattern 1). Note the requirement above to transmit five repeats of the Idle Pattern after receiving ACK from the Sink.



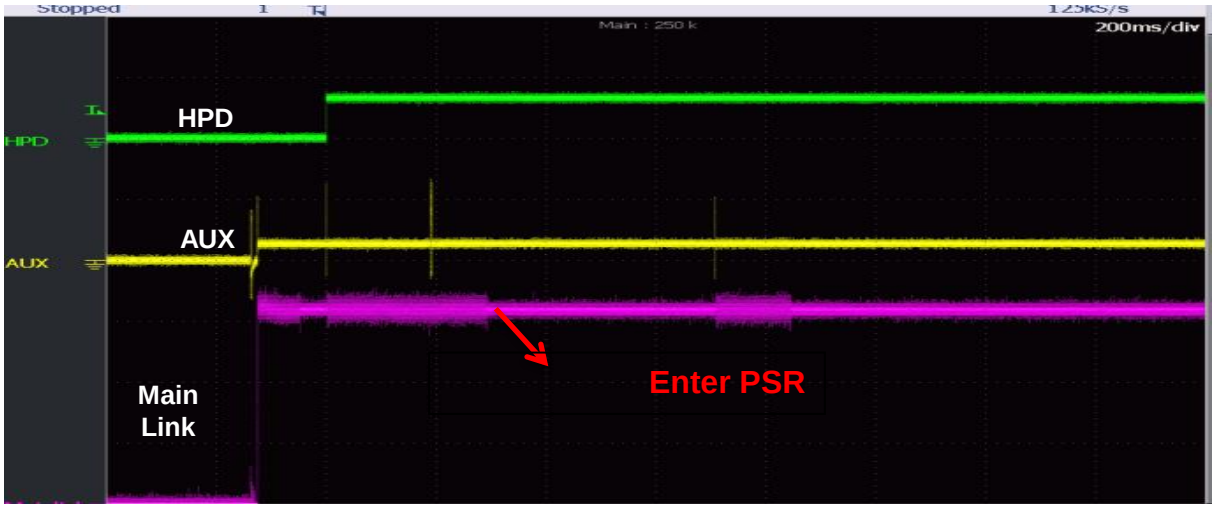
-. The below waveform is the issued case.



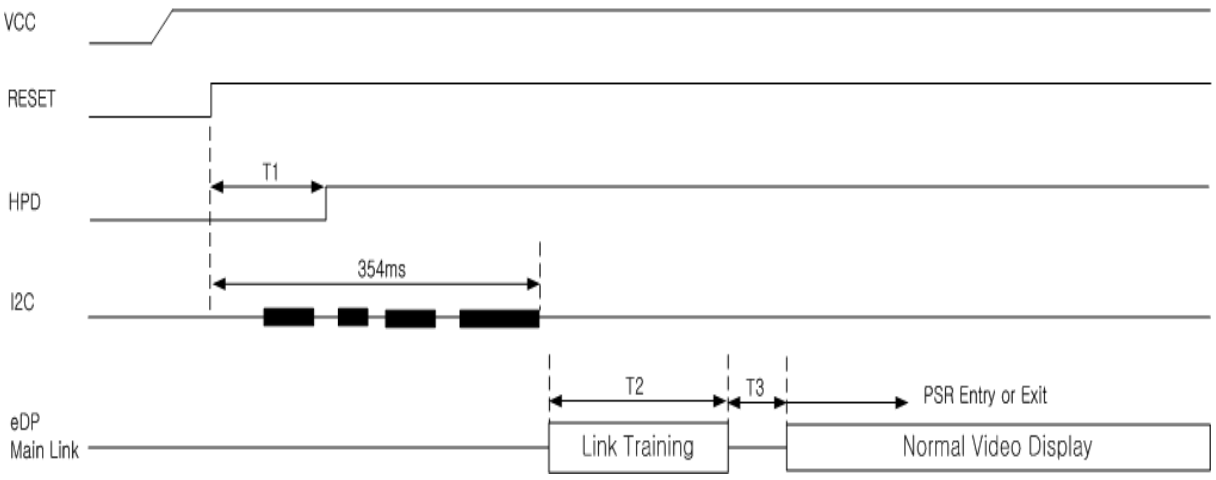
Define	If link training is not required, the source must begin transmitting data on the ML prior to the wake AUX wake-up command.

APPENDIX A. LGD Proposal for eDP Interface Design Guide

8	1st time PSR Entry after Power on



< Issue waveform >



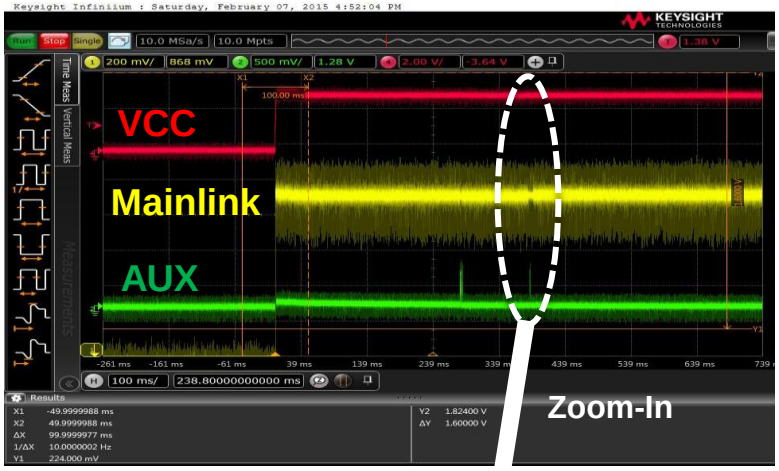
< solution waveform >

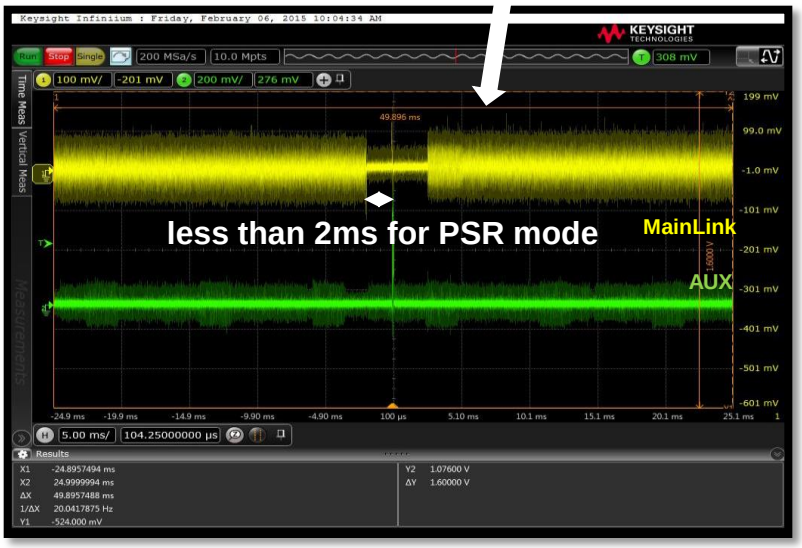
1. **According to test, t-con is stable T3(83.3ms=5frame) after Link Training Done.**

Define	After power(Vcc) on, the DP link is not stable, so the source try to PSR entry at 83.3ms after Link Training Done.

APPENDIX A. LGD Proposal for eDP Interface Design Guide

9	PSR Period Issue



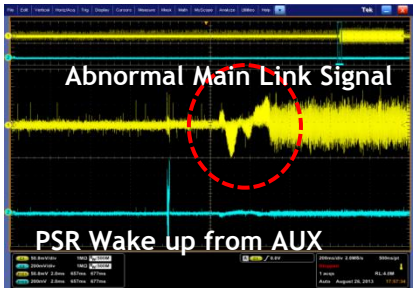


1. When issue is happened, system go to PSR mode for very short time.
2. If PSR active period is shorter than 1frame(16.67ms), T-Con can not go to the standby mode for PSR exit.

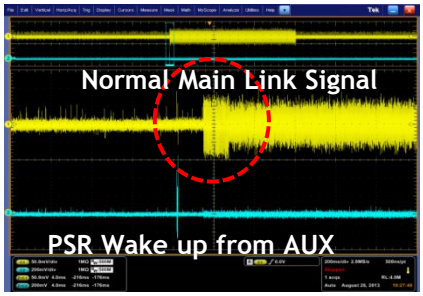
Define	When GPU go to the PSR mode, the source must hold the main link off over than 1frame.

APPENDIX A. LGD Proposal for eDP Interface Design Guide

10	Main Link Noise at PSR Exit



[Abnormal Main Link Noise]



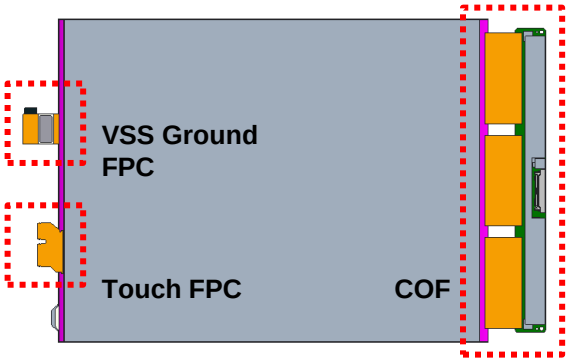
[Normal Main Link Signal]

Define	Main Link Noise at PSR Exit mode can be a cause abnormal display.

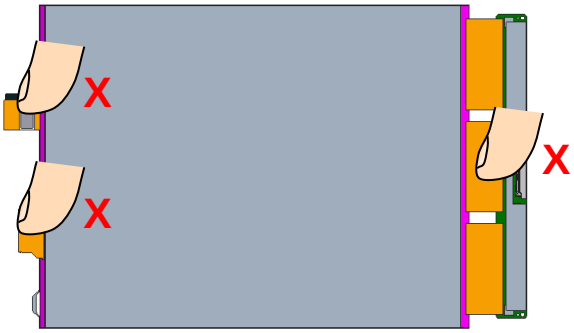
APPENDIX B. LGD Proposal for System Design

01	COF, FPC crack risk by external stress

1. Careful handling is required against COF and FPC Crack Risk
   - Do not give external force and stress to FPC and COF directly during Inspection and Assembly
   - Handle FPC/COF bending Area carefully to prevent damage



[Handling Caution Area]

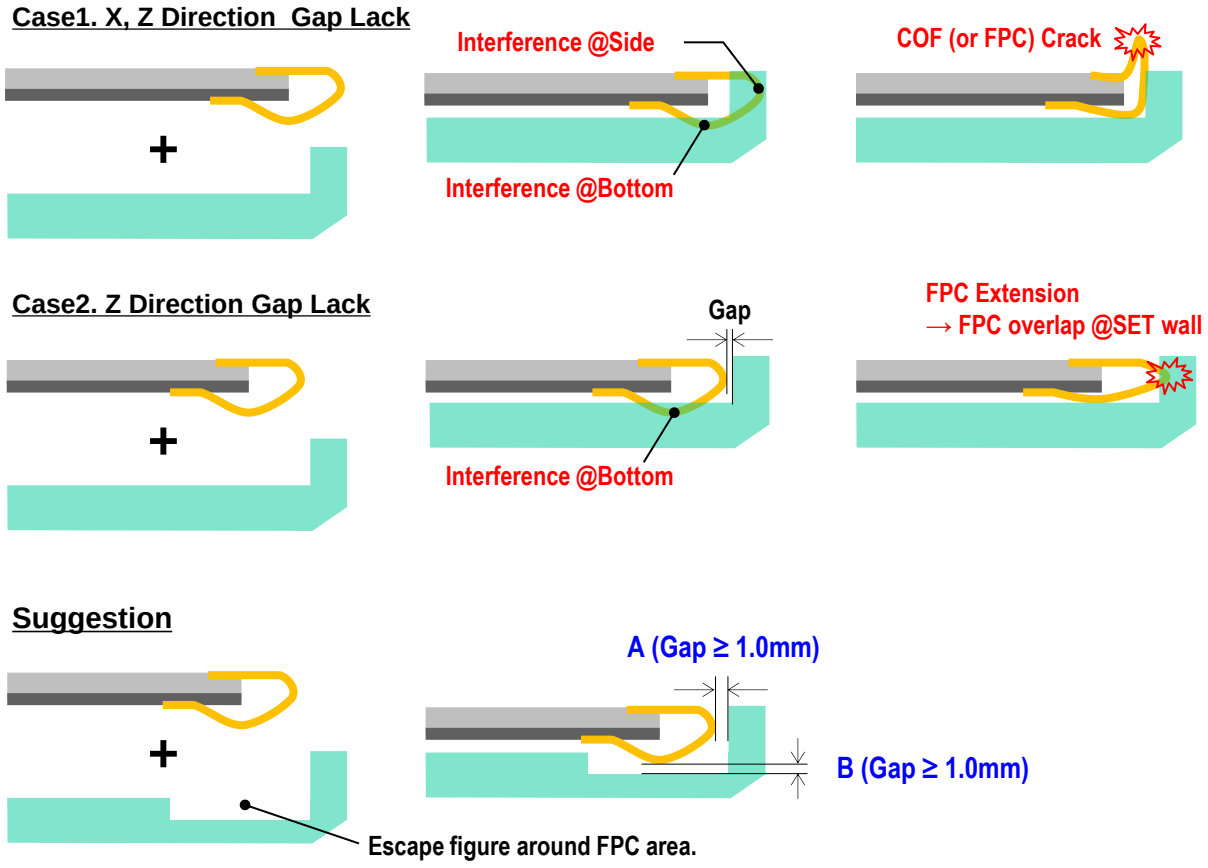


APPENDIX B. LGD Proposal for System Design

02	System gap near COF, FPC area

1. System Gap suggestion

- FPC and COF can be easily cracked by interference between FPC and frame during repetitive external shock or vibration.
- FPC crack can be improved by add escape figure at system frame and the gap is recommended to keep more than 1.0mm

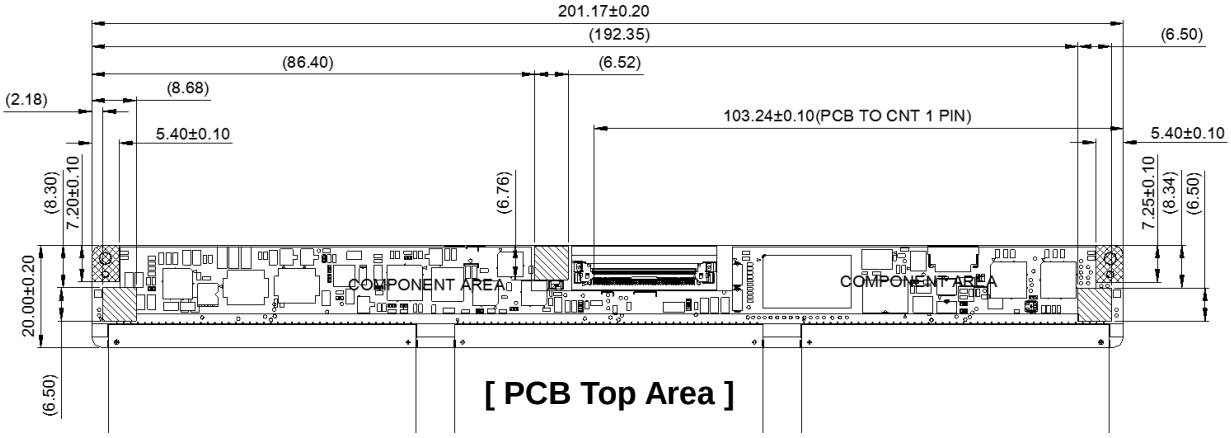


	FO module dimension	Gap (SET wall ~ COF)
A (X-Direction)	Max. Outline (including COF bending loop)	Min. 1.0mm
B (Z-Direction)	Max. Thickness (including COF floating)	Min. 1.0mm

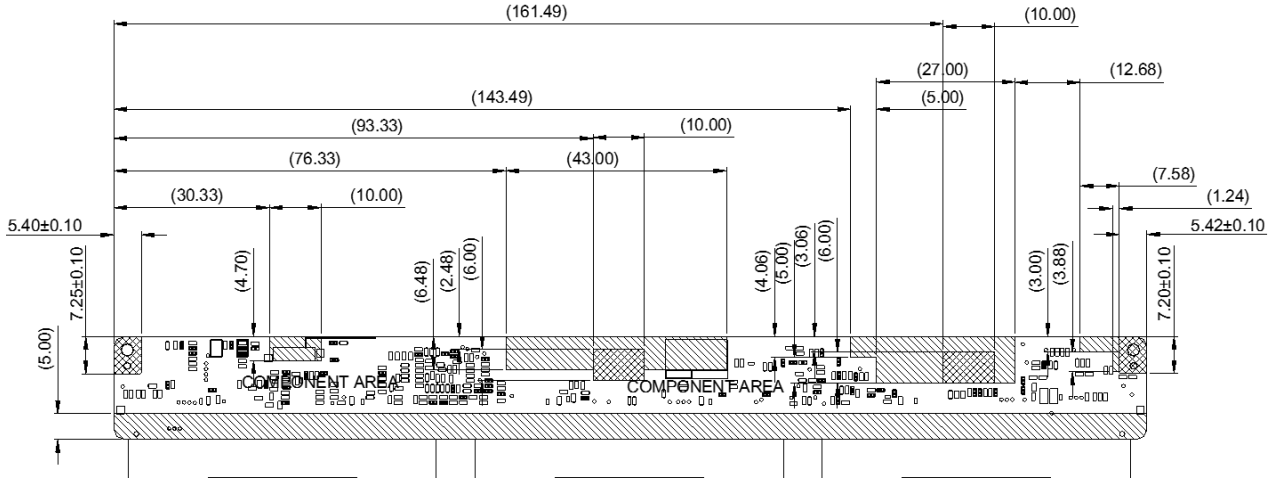
APPENDIX B. LGD Proposal for PCB Shielding Guide

03	Short Risk by Conductive PCB Shielding

1. Conductive area of PCB Shielding Cover can not be attached on circuit parts and test points.



[PCB Top Area]



[PCB Bottom Area]

NOTE

1. The hatch " ▨ " On PCB is no Component area & Any conductive tape must be not attached.
2. The hatch " ▨ " On PCB is GND area & Possible to attach conductive tape.
3. Any Conductive tape must be not attached on the Component Area.

APPENDIX C. Enhanced Extended Display Identification Data (EEDID™) 1/3

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
Header	0	**00**	Header	**00**	00000000
	1	**01**	Header	**FF**	11111111
	2	**02**	Header	**FF**	11111111
	3	**03**	Header	**FF**	11111111
	4	**04**	Header	**FF**	11111111
	5	**05**	Header	**FF**	11111111
	6	**06**	Header	**FF**	11111111
	7	**07**	Header	**00**	00000000
Vendor / Product EDID Version	8	**08**	ID Manufacture Name LGD	**30**	00110000
	9	**09**	ID Manufacture Name	**E4**	11100100
	10	**0A**	ID Product Code 064Dh	**4D**	01001101
	11	**0B**	(Hex. LSB first)	**06**	00000110
	12	**0C**	ID Serial No. - Optional ("00h" If not used, Number Only and LSB First)	**00**	00000000
	13	**0D**	ID Serial No. - Optional ("00h" If not used, Number Only and LSB First)	**00**	00000000
	14	**0E**	ID Serial No. - Optional ("00h" If not used, Number Only and LSB First)	**00**	00000000
	15	**0F**	ID Serial No. - Optional ("00h" If not used, Number Only and LSB First)	**00**	00000000
	16	**10**	Week of Manufacture - Optinal 00 weeks	**00**	00000000
	17	**11**	Year of Manufacture 2020 years	**1E**	00011110
	18	**12**	EDID structure version # = 1	**01**	00000001
	19	**13**	EDID revision # = 4	**04**	00000100
Display Parameters	20	**14**	Video input Definition = Input is a Digital Video signal Interface , Colo Bit Depth : 8 Bits per Primary Color , Digital Video Interface Standard Supported: DisplayPort is supported	**A5**	10100101
	21	**15**	Horizontal Screen Size (Rounded cm) = 20 cm	**14**	00010100
	22	**16**	Vertical Screen Size (Rounded cm) = 27 cm	**1B**	00011011
	23	**17**	Display Transfer Characteristic (Gamma) = (gamma*100)-100 = Example:(2.2*100)-100=120	**78**	01111000
	24	**18**	Feature Support [Display Power Management(DPM) : Standby Mode is not supported, Suspend Mode is not supported, Active Off = Very Low Power is not supported ,Supportted Color Encoding Formats : RGB 4:4:4 ,Other Feature Support Flags : No_sRGB, Preferred Timing Mode, No_Display is continuous frequency (Multi-mode_Base EDID and Extension Block).]	**02**	00000010
Panel Color Coordinates	25	**19**	Red/Green Low Bits (RxRy/GxGy)	**02**	00000010
	26	**1A**	Blue/White Low Bits (BxBy/WxWy)	**D5**	11010101
	27	**1B**	Red X Rx = 0.695	**B2**	10110010
	28	**1C**	Red Y Ry = 0.305	**4E**	01001110
	29	**1D**	Green X Gx = 0.176	**2D**	00101101
	30	**1E**	Green Y Gy = 0.740	**BD**	10111101
	31	**1F**	Blue X Bx = 0.140	**23**	00100011
	32	**20**	Blue Y By = 0.056	**0E**	00001110
	33	**21**	White X Wx = 0.313	**50**	01010000
	34	**22**	White Y Wy = 0.329	**54**	01010100
Established Timings	35	**23**	Established timing 1 (Optional_00h if not used)	**00**	00000000
	36	**24**	Established timing 2 (Optional_00h if not used)	**00**	00000000
	37	**25**	Manufacturer's timings (Optional_00h if not used)	**00**	00000000
Standard Timing ID	38	**26**	Standard timing ID1 (Optional_01h if not used)	**01**	00000001
	39	**27**	Standard timing ID1 (Optional_01h if not used)	**01**	00000001
	40	**28**	Standard timing ID2 (Optional_01h if not used)	**01**	00000001
	41	**29**	Standard timing ID2 (Optional_01h if not used)	**01**	00000001
	42	**2A**	Standard timing ID3 (Optional_01h if not used)	**01**	00000001
	43	**2B**	Standard timing ID3 (Optional_01h if not used)	**01**	00000001
	44	**2C**	Standard timing ID4 (Optional_01h if not used)	**01**	00000001
	45	**2D**	Standard timing ID4 (Optional_01h if not used)	**01**	00000001
	46	**2E**	Standard timing ID5 (Optional_01h if not used)	**01**	00000001
	47	**2F**	Standard timing ID5 (Optional_01h if not used)	**01**	00000001
	48	**30**	Standard timing ID6 (Optional_01h if not used)	**01**	00000001
	49	**31**	Standard timing ID6 (Optional_01h if not used)	**01**	00000001
	50	**32**	Standard timing ID7 (Optional_01h if not used)	**01**	00000001
	51	**33**	Standard timing ID7 (Optional_01h if not used)	**01**	00000001
	52	**34**	Standard timing ID8 (Optional_01h if not used)	**01**	00000001
	53	**35**	Standard timing ID8 (Optional_01h if not used)	**01**	00000001

APPENDIX C. Enhanced Extended Display Identification Data (EEDID™) 2/3

	Byte (Dec)	Byte (Hex)	Field Name and Comments		Value (Hex)	Value (Bin)
Timing Descriptor #1	54	**36**	Pixel Clock/10,000 (LSB)	215 MHz @ 60 Hz	**FC**	11111100
	55	**37**	Pixel Clock/10,000 (MSB)		**53**	01010011
	56	**38**	Horizontal Active (HA) (lower 8 bits)	1536 pixels	**00**	00000000
	57	**39**	Horizontal Blanking (HB) (lower 8 bits)	160 pixels	**A0**	10100000
	58	**3A**	Horizontal Active (HA) / Horizontal Blanking (HB) (upper 4:4bits)		**60**	01100000
	59	**3B**	Vertical Avtive (VA)	2048 lines	**00**	00000000
	60	**3C**	Vertical Blanking (VB) (DE Blanking typ.for DE only panels)	64 lines	**40**	01000000
	61	**3D**	Vertical Active (VA) / Vertical Blanking (VB) (upper 4:4bits)		**80**	10000000
	62	**3E**	Horizontal Front Porch in pixels (HF) (lower 8 bits)	48 pixels	**30**	00110000
	63	**3F**	Horizontal Sync Pulse Width in pixels (HS) (lower 8 bits)	32 pixels	**20**	00100000
	64	**40**	Vertical Front Porch in lines (VF) : Vertical Sync Pluse Width in lines (VS) (lower 4 bits)	3 lines : 10 lines	**3A**	00111010
	65	**41**	Horizontal Front Porch/ Sync Pulse Width/ Vertical Front Porch/ Sync Pulse Width (upper 2bits)		**00**	00000000
	66	**42**	Horizontal Vedio Image Size (mm) (lower 8 bits)	203 mm	**CB**	11001011
	67	**43**	Vertical Vedio Image Size (mm) (lower 8 bits)	270 mm	**0E**	00001110
	68	**44**	Horizontal Image Size / Vertical Image Size (upper 4 bits)		**01**	00000001
	69	**45**	Horizontal Border = 0 (Zero for Notebook LCD)		**00**	00000000
	70	**46**	Vertical Border = 0 (Zero for Notebook LCD)		**00**	00000000
	71	**47**	Non-Interlace, Normal display, no stereo, Digital Separate [Vsync_NEG, Hsync_POS (outside of V-sync)]		**1A**	00011010
Timing Descriptor #2	72	**48**	Flag		**00**	00000000
	73	**49**	Flag		**00**	00000000
	74	**4A**	Flag		**00**	00000000
	75	**4B**	Data Type Tag (Descriptor Defined by manufacturer)		**00**	00000000
	76	**4C**	Flag		**00**	00000000
	77	**4D**	Descriptor Defined by manufacturer		**00**	00000000
	78	**4E**	Descriptor Defined by manufacturer		**00**	00000000
	79	**4F**	Descriptor Defined by manufacturer		**00**	00000000
	80	**50**	Descriptor Defined by manufacturer		**00**	00000000
	81	**51**	Descriptor Defined by manufacturer		**00**	00000000
	82	**52**	Descriptor Defined by manufacturer		**00**	00000000
	83	**53**	Descriptor Defined by manufacturer		**00**	00000000
	84	**54**	Descriptor Defined by manufacturer		**00**	00000000
	85	**55**	Descriptor Defined by manufacturer		**00**	00000000
	86	**56**	Descriptor Defined by manufacturer		**00**	00000000
	87	**57**	Descriptor Defined by manufacturer		**00**	00000000
	88	**58**	Descriptor Defined by manufacturer		**00**	00000000
	89	**59**	Descriptor Defined by manufacturer		**00**	00000000
Timing Descriptor #3	90	**5A**	Flag		**00**	00000000
	91	**5B**	Flag		**00**	00000000
	92	**5C**	Flag		**00**	00000000
	93	**5D**	Data Type Tag (Alphanumeric Data String (ASCII String))		**FE**	11111110
	94	**5E**	Flag		**00**	00000000
	95	**5F**	Alphanumeric Data String (ASCII String)	L	**4C**	01001100
	96	**60**	Alphanumeric Data String (ASCII String)	G	**47**	01000111
	97	**61**	Alphanumeric Data String (ASCII String)		**20**	00100000
	98	**62**	Alphanumeric Data String (ASCII String)	D	**44**	01000100
	99	**63**	Alphanumeric Data String (ASCII String)	i	**69**	01101001
	100	**64**	Alphanumeric Data String (ASCII String)	s	**73**	01110011
	101	**65**	Alphanumeric Data String (ASCII String)	p	**70**	01110000
	102	**66**	Alphanumeric Data String (ASCII String)	l	**6C**	01101100
	103	**67**	Alphanumeric Data String (ASCII String)	a	**61**	01100001
	104	**68**	Alphanumeric Data String (ASCII String)	y	**79**	01111001
	105	**69**	Manufacturer P/N(If<13 char--> 0Ah, then terminate with ASC II code 0Ah,set remaining char = 20h)		**0A**	00001010
	106	**6A**	Manufacturer P/N(If<13 char--> 0Ah, then terminate with ASC II code 0Ah,set remaining char = 20h)		**20**	00100000
	107	**6B**	Manufacturer P/N(If<13 char--> 0Ah, then terminate with ASC II code 0Ah,set remaining char = 20h)		**20**	00100000

APPENDIX C. Enhanced Extended Display Identification Data (EEDID™) 3/3

	Byte (Dec)	Byte (Hex)	Field Name and Comments		Value (Hex)	Value (Bin)
Timing Descriptor #4	108	**6C**	Flag		**00**	00000000
	109	**6D**	Flag		**00**	00000000
	110	**6E**	Flag		**00**	00000000
	111	**6F**	Data Type Tag (Alphanumeric Data String (ASCII String))		**FE**	11111110
	112	**70**	Flag		**00**	00000000
	113	**71**	Alphanumeric Data String (ASCII String)	L	**4C**	01001100
	114	**72**	Alphanumeric Data String (ASCII String)	P	**50**	01010000
	115	**73**	Alphanumeric Data String (ASCII String)	1	**31**	00110001
	116	**74**	Alphanumeric Data String (ASCII String)	3	**33**	00110011
	117	**75**	Alphanumeric Data String (ASCII String)	3	**33**	00110011
	118	**76**	Alphanumeric Data String (ASCII String)	Q	**51**	01010001
	119	**77**	Alphanumeric Data String (ASCII String)	X	**58**	01011000
	120	**78**	Alphanumeric Data String (ASCII String)	1	**31**	00110001
	121	**79**	Alphanumeric Data String (ASCII String)	-	**2D**	00101101
	122	**7A**	Alphanumeric Data String (ASCII String)	E	**45**	01000101
	123	**7B**	Alphanumeric Data String (ASCII String)	P	**50**	01010000
	124	**7C**	Alphanumeric Data String (ASCII String)	A	**41**	01000001
	125	**7D**	Alphanumeric Data String (ASCII String)	1	**31**	00110001
Checksum	126	**7E**	Extension flag (# of optional 128 panel ID extension block to follow, Typ = 0)		**00**	00000000
	127	**7F**	Check Sum (The 1-byte sum of all 128 bytes in this panel ID block shall = 0)		**EB**	11101011